TI Extensa 61X Series
(AcerNote 370P) Notebook

Service Guide

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About this Manual

Purpose

This service guide contains reference information for the Extensa 610 notebook computer. It gives the system and peripheral specifications, shows how to identify and solve system problems and explains the procedure for removing and replacing system components. It also gives information for ordering spare parts.

Manual Structure

This service guide consists of four chapters and seven appendices as follows:

Chapter 1 System Introduction

This chapter gives the technical specifications for the notebook and its peripherals.

Chapter 2 Major Chip Descriptions

This chapter lists the major chips used in the notebook and includes pin descriptions and related diagrams of these chips.

Chapter 3 BIOS Setup Information

This chapter includes the system BIOS information, focusing on the BIOS setup utility.

Chapter 4 Disassembly and Unit Replacement

This chapter tells how to disassemble the notebook and replace components.

Appendix A Model Number Definition

This appendix lists the model number definition of this notebook model series.

Appendix B Exploded View Diagram

This appendix shows the exploded view diagram of the notebook.

Appendix C Spare Parts List

This appendix contains spare parts information.

Appendix D Schematics

This appendix contains the schematic diagrams of the notebook.

Appendix E BIOS POST Checkpoints

This appendix lists all the BIOS POST checkpoints.

Appendix F Technical Bulletins and Updates

This appendix reserves a space for technical bulletins and future updates.

Appendix G Forms

This appendix contains standard forms that can help improve customer service.

Related product information

AcerNote 370P User's Manual contains system description and general operating instructions.
M1521, M1523 and M7101 Data Sheets contain information on the Acer chips.
C&T 65550 Data Sheet contains detailed information on the Chips & Tech. VGA controller.
TI PCI1131 Data Sheet contains detailed information on the Texas Instrument PCMCIA controller.
NS87336VJG Data Sheet contains detailed information on the NS super I/O controller.
YMF715 Data Sheet contains detailed information on the Yamaha YMF715 audio controller.
T62.062.C, T62.061.C, T62.064.C, and T62.066.C Data Sheets contain detailed information on the Ambit components.

Conventions

The following are the conventions used in this manual:

`Text entered by user`	Represents text input by the user.
`Screen messages`	Denotes actual messages that appear onscreen.
	**NOTE** Gives bits and pieces of additional information related to the current topic.
	**WARNING** Alerts you to any damage that might result from doing or not doing specific actions.
	**CAUTION** Gives precautionary measures to avoid possible hardware or software problems.
	**IMPORTANT** Reminds you to do specific actions relevant to the accomplishment of procedures.
	**TIP** Tells how to accomplish a procedure with minimum steps through little shortcuts.

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Chapter 1 System Introduction

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System Introduction

This chapter introduces the notebook, its features, components and specifications.

1.1 Overview

The notebook was designed with the user in mind. The figure below shows the notebook with the display open.

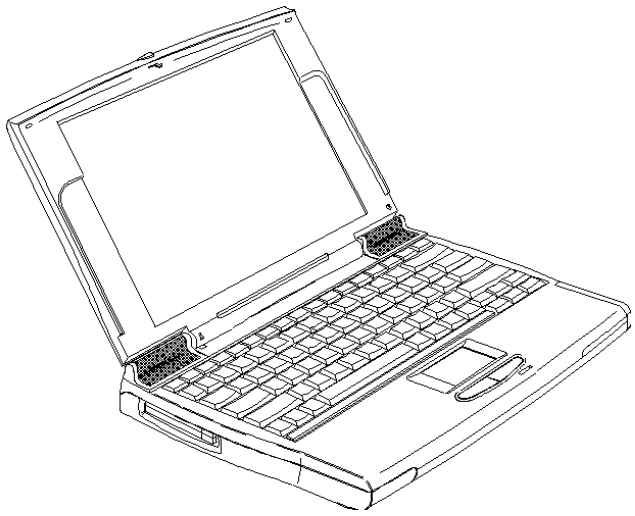


Figure 1-1 Notebook

1.1.1 Features

Here are just a few of the notebook's many features:

Performance

- High-end Pentium microprocessor
- Support 64-bit main memory and external (L2) cache memory
- Large LCD display (DualScan STN and TFT active matrix.)
- PCI local bus video with graphics acceleration and 1MB video RAM boost video performance
- Internal 3.5-inch floppy drive or CD-ROM drive
- High-capacity, Enhanced-IDE hard disk
- Lithium-Ion or Nickel Metal-Hydride battery pack
- Power management system with standby and hibernation power saving modes

Multimedia

- 16-bit stereo audio with software wavetable
- Built-in dual speakers
- Ultra-slim, high-speed CD-ROM drive[1]

Human-centric Design and Ergonomics

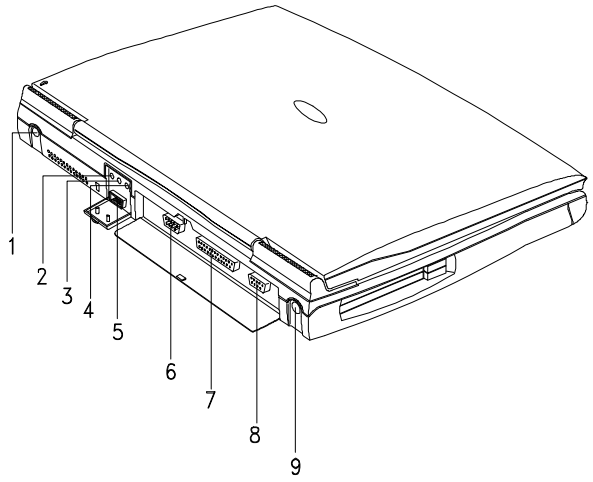
- Lightweight and slim
- Sleek, smooth and stylish design
- Full-sized keyboard
- Wide and curved palm rest
- Centrally-located touchpad pointing device

Expansion

- PC card (formerly PCMCIA) slots (two type II/I or one type III) with ZV (Zoomed Video) port support
- Upgradeable memory, hard disk, CPU

1 Some areas or regions may not offer models with a built-in CD-ROM drive.

1.1.2 Rear Ports



1 DC-in Port
2 Microphone-in Port
3 Line-in Port
4 Line-out Port
5 External Floppy Drive Connector
6 Serial Port
7 Parallel Port
8 External CRT Port
9 PS/2 Port

Figure 1-2 Rear Ports

The following table describes these ports.

Table 1-1 Port Descriptions

#	Icon	Port	Connects to...
1		DC-in Port	AC adapter and power outlet
2		Microphone-in Port	External 3.5mm minijack condenser microphone
3		Line-in Port	Line-in device (e.g., CD player, stereo walkman)
4		Line-out Port	Line-out device (e.g., speakers, headphones)
5		External Floppy Drive Connector	External floppy drive
6		Serial Port	Serial device (e.g., serial mouse)
7		Parallel Port	Parallel device (e.g., parallel printer)
8		External CRT port	Monitor (up to 1024x768, 256-colors)
9		PS/2 Port	PS/2-compatible device (e.g., PS/2 keyboard, keypad, mouse)

1.1.3 Indicator Light

A two-way indicator light is found on the inside and outside of the display. See figure below.

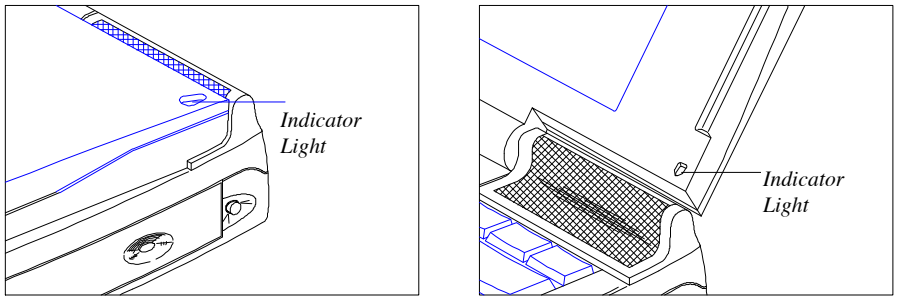


Figure 1-3 Indicator Light

This two-way indicator light allows you to see the notebook status when the display is open or closed. The indicator serves both as a power and battery-charging indicator. See Table 1-2.

Table 1-2 Indicator Status Descriptions

Indicator Status	Power Switch	Condition
Green	On	Charged battery is installed **or** a power AC adapter is connected to the notebook.
Red	Off	Battery is installed and a powered AC adapter is connected to the notebook and charging the battery (rapid charge mode).
Orange	On	Battery is installed and a powered AC adapter is connected to the notebook and charging the battery (charge-in-use mode).
Flashing	On	Battery is running low on power and no AC adapter is connected to the notebook.

1.1.4 System Specifications Overview

Table 1-3 System Specifications

Item	Standard	Optional
Microprocessor	Intel Pentium™ processor (Intel P54CSLM 120/133/150 MHz)	Intel P55CLM - 133/150 with MMX
System memory	8MB / 16MB Dual 64-bit memory banks	Expandable to 64MB using 8, 16 and 32MB soDIMMs
Flash ROM BIOS	256KB	
Data storage devices CD-ROM model FDD model	Removable 12.5mm, 2.5-inch, 1.0GB Enhanced-IDE hard disk Internal 15mm, 5.25-inch high-speed CD-ROM drive Internal 3.5-inch, 1.44MB floppy drive	1+GB Enhanced-IDE hard disk drive External 3.5-inch, 1.44MB diskette drive
Display	DualScan STN or TFT active matrix, 800x600, 256 colors (SVGA)	Up to 1024x768, 256-color ultra-VGA monitor LCD projection panel
Video	PCI local bus video with graphics accelerator and 1MB video RAM	
Audio	16-bit stereo audio; built-in dual speakers; separate audio ports	
Keyboard and pointing device	84-/85-/88-key with Windows 95 keys Touchpad (centrally-located on palmrest)	101-/102-key, PS/2-compatible keyboard or 17-key numeric keypad External serial or PS/2 mouse or similar pointing device
I/O ports	One 9-pin RS-232 serial port (UART16550-compatible) One 25-pin parallel port (EPP/ECP-compliant) One 15-pin CRT port One 6-pin PS/2 keypad/ keyboard/mouse connector One type III or two type II PC Card slot(s) with ZV port support One external FDD port	Serial mouse, printer or other serial devices Parallel printer or other parallel devices Up to a 1024x768, 256-color ultra-VGA monitor 17-key numeric keypad, PS/2 keyboard or mouse LAN card or other PC cards External diskette drive

Table 1-3 System Specifications (continued)

Item	Standard	Optional
I/O ports (continued)	One 3.5mm minijack mic-in port One 3.5mm minijack line-in port One 3.5mm minijack line-out port	Microphone Audio CD player or other line-in devices Speakers or headphones
Operating system	Windows 95	Windows 3.1
Weight FDD model CD-ROM model	(includes battery) 2.6 kg. (5.7 lbs.) 2.8 kg. (6.2 lbs.)	
Dimensions (main footprint)	W x D x H 306mm x 228mm x 46mm (12.05" x 8.98" x 1.81")	
Temperature Operating Non-operating	 10ºC ~ 35ºC -20ºC ~ 60ºC	
Humidity Operating Non-operating	(non-condensing) 20% ~ 80% 20% ~ 80%	
AC adapter	100~240 Vac, 50~60 Hz, 45W autosensing AC adapter	Extra AC adapter
Battery pack		
Lithium-Ion	4-5 hr. (rapid-charge) 6-8 hr. (charge-in-use)	Extra battery pack External battery charger/discharger
Nickel Metal-Hydride battery	2-2.5 hr. (rapid-charge) 5.5-6.5 hr. (charge-in-use)	Extra battery pack External battery charger/discharger

1.2 System Board Layout

1.2.1 Main Board (PCB No: 96149-SC)

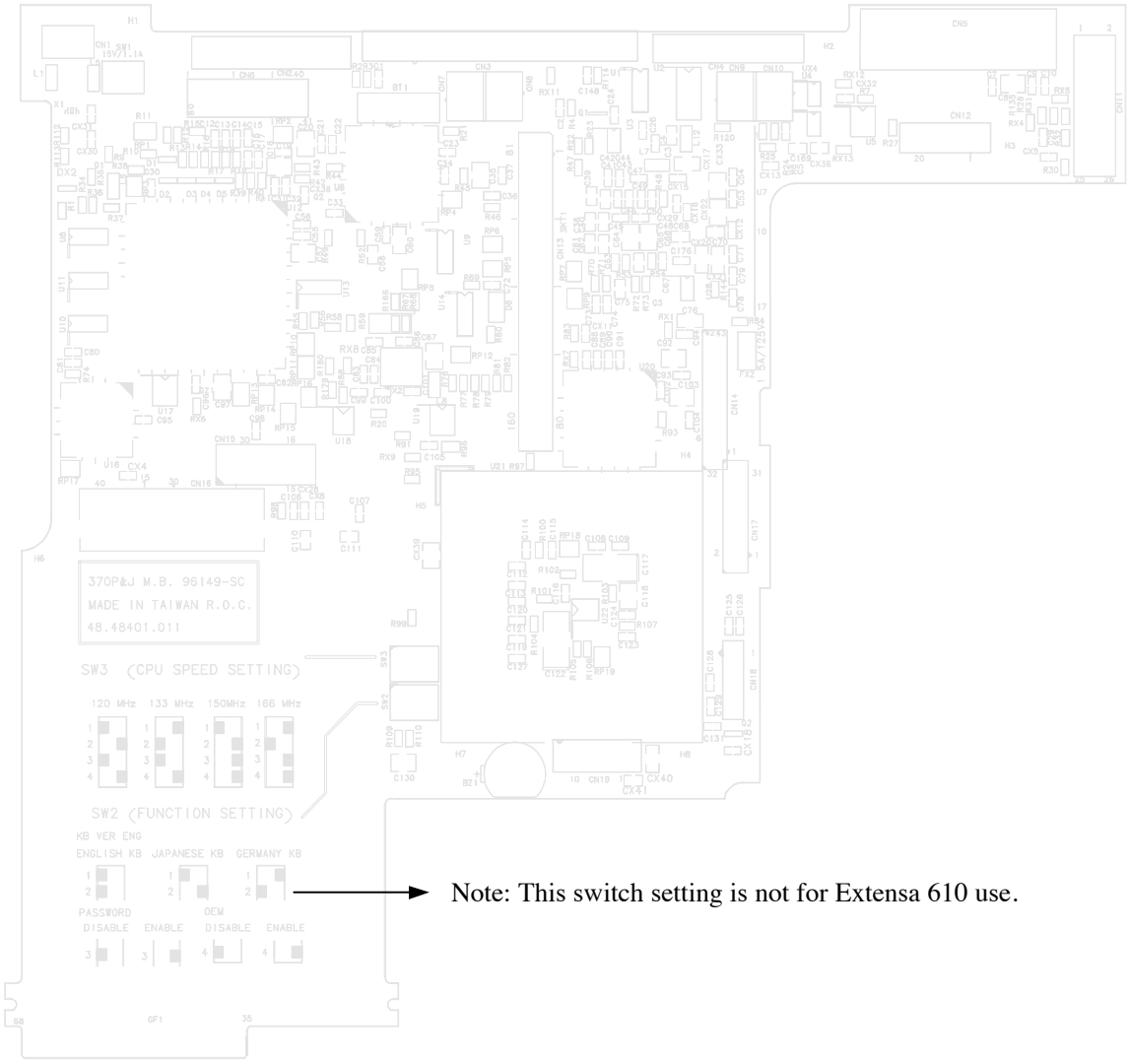


Figure 1-4 Main Board Layout (Top Side)

Figure 1-5 Main Board Layout (Bottom Side)

1.2.2 Audio Connection Board (PCB No:96467-1)

Figure 1-6 Audio Connection Board Layout (Top Side)

1.2.3 Battery Connection Board (PCB No:95498-1)

Figure 1-7 Battery Connection Board Layout (Top Side)

Figure 1-8 Battery Connection Board Layout (Bottom Side)

1.2.4 HDD Connection Board (PCB No:96463-1)

Figure 1-9 HDD Connection Board Layout (Top Side)

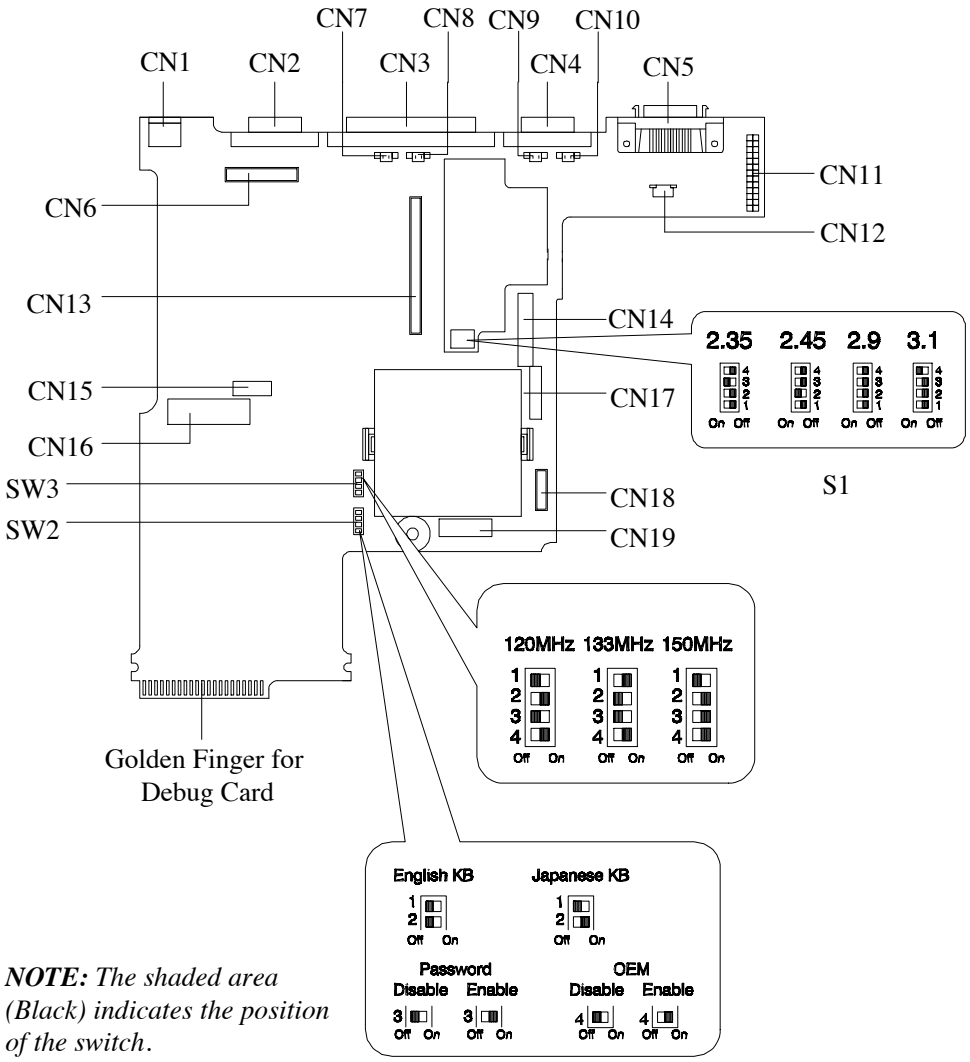
Figure 1-10 HDD Connection Board Layout (Bottom Side)

1.2.5 Keyboard Connection Board (PCB No: 96465-1)

Figure 1-11 Keyboard Connection Board Layout (Top Side)

Figure 1-12 Keyboard Connection Board Layout (Bottom Side)

1.3 Jumpers and Connectors



NOTE: *The shaded area (Black) indicates the position of the switch.*

CN1 External PS/2 keyboard/mouse port
CN2 VGA port
CN3 Parallel port
CN4 Serial port
CN5 External floppy drive port
CN6 LCD Connector
CN7 Audio speaker connector (left)
CN8 LCD cover switch connector
CN9 Fan connector
CN10 Audio speaker connector (right)
CN11 Charger Connector
CN12 Audio Board Connector
CN13 PCMCIA socket connector
CN14 Diskette Drive connector
CN15 HDD Connector
CN16 Keyboard connector
CN17 CD-ROM connector
CN18 Battery pack connector
CN19 Track Point Board Connector
S1 CPU Voltage Setting
SW2 Function Setting
SW3 CPU Speed Setting

Figure 1-13 Jumpers and Connectors (Top View)

Table 1-4 CPU Voltage (S1) Settings

CPU Voltage	2.35V	2.45V	2.9V	3.1V
Switch 1	Off	Off	Off	Off
Switch 2	Off	On	Off	Off
Switch 3	On	Off	Off	Off
Switch 4	Off	Off	Off	On

Table 1-5 CPU Speed (SW3) Settings

CPU Speed	120MHz	133MHz	150MHz
Switch 1	Off	On	Off
Switch 2	On	Off	On
Switch 3	Off	Off	On
Switch 4	On	On	On

Table 1-6 Multi-Function Switch (SW2) Settings

Switch		ON	OFF
1	**Keyboard Type (Default OFF)**	-	-
2	**Keyboard Type**	88-key (Japan keyboard)	84/85-key (U.S. keyboard)
3	**Password**	Bypass	Check
4	**Generic boot-up screen show on screen in POST**	No	Yes

1.4 Hardware Configuration and Specification

1.4.1 Memory Address Map

Table 1-7 Memory Address Map

Address Range	Definition	Function
000000 - 09FFFF	640 KB memory	Base memory
0A0000 - 0BFFFF	128 KB video RAM	Reserved for graphics display buffer
0C0000 - 0CBFFF	Video BIOS	Video BIOS
0E0000 - 0EFFFF 0F0000 - 0FFFFF	128 KB system BIOS	System BIOS System BIOS
10000 - 7FFFF 80000 - 27FFF	Extended memory	Onboard Memory SIMM memory
FE0000 - FFFFFF	256 KB system ROM	Duplicate of code assignment at 0E0000-0FFFFF

1.4.2 Interrupt Channel Map

Table 1-8 Interrupt Channel Map

Priority	Interrupt Number	Interrupt Source
1	SMI	Power management unit
2	NMI	Parity error detected, I/O channel error
3	IRQ 0	Interval timer, counter 0 output
4	IRQ 1	Keyboard
	IRQ 2	Interrupt from controller 2 (cascade)
5	IRQ 8	Real-time clock
6	IRQ 9	Cascaded to INT 0AH (IRQ 2)
7	IRQ 10	Audio (option) / PCMCIA
8	IRQ 11	Audio (option) / PCMCIA
9	IRQ 12	PS/2 mouse
10	IRQ 13	INT from coprocessor
11	IRQ 14	Hard disk controller
12	IRQ 15	CD-ROM controller
13	IRQ 3	Serial communication port 2
14	IRQ 4	Serial communication port 1
15	IRQ 5	Parallel port (option) / Audio
16	IRQ 6	Diskette controller
17	IRQ 7	Parallel port (option)

A PCMCIA card can use IRQ 3, 4, 5, 7, 9 and 11 as long as it does not conflict with the interrupt address of any other device.

1.4.3 DMA Channel Map

Table 1-9 DMA Channel Map

Controller	Channel	Address	Function
1	0	0087	Audio (option)/ECP(option)

1	1	0083	Audio
1	2	0081	Diskette
1	3	0082	Audio (option)/ECP(option)
2	4	Cascade	Cascade
2	5	008B	-
2	6	0089	Spare
2	7	008A	-

1.4.4 I/O Address Map

Table 1-10 I/O Address Map

Address Range	Device
000 - 00F	DMA controller-1
020 - 021	Interrupt controller-1
040 - 043	Timer 1
048 - 04B	Timer 2
060 - 064	Keyboard controller 38802 chip select
070 - 071	Real-time clock and NMI mask
080 - 08F	DMA page register
0A0 - 0A1	Interrupt controller-2
0C0 - 0DF	DMA controller-2
170 - 177	CD-ROM
178, 17A	M7101 registers
1F0 - 1F7	Hard disk select
3F6, 3F7	
220 - 22F, 240 - 24F	Audio (option) - default
300 - 301, 330 - 331	Audio (option)
370 - 371, 388 - 38F	Audio (option)
530 - 537, E80 - E89	Audio (option)
278 - 27F	Parallel port 3
2E8 - 2EF	COM 4
2F8 - 2FF	COM 2
378, 37A	Parallel port 2
3BC - 3BE	Parallel port 1
3B4, 3B5, 3BA	Video subsystem
3C0 - 3C5	
3C6 - 3C9	Video DAC
3C0 - 3CF	Enhanced graphics display
3D0 - 3DF	Color graphics adapter
3E0 - 3E1	PCMCIA controller
3E8 - 3EF	COM3
3F0 - 3F7	Floppy disk controller
3F8 - 3FF	COM 1
CF8 - CFF	PCI configuration register

1.4.5 M7101 GPIO (General Purpose I/O) Port Definition

Table 1-11 M7101 GPIO Port Definition

Item	Description
GPIOA2	Smart inverter contrast counter control
GPIOA3	0: Normal operation of system 1: Shutdown system
GPIOA4	Serial data on X24C02
GPIOA5	Battery gauge communication control
GPIOA6	Battery data line
GPIOA7	Thermal sensor data line
GPIOC6	VGA thermal sensor data line
GPIOC7	0: VGA chip standby mode 1: Normal operation
Register E0h bit 8	Serial clock on X24C02
Register E0h bit 9	0: Disable 12V for flash ROM 1: Enable 12V for flash ROM
Register E0h bit 10	0: 3 mode FDD 1: Normal
Register E0h bit 11	Thermal sensor clock line
Register E0h bit 12	Thermal sensor reset
Register E0h bit 13	0: Enable battery LED 1: Disable battery LED
Register E0h bit 14	0: Disable audio amplifier 1: Enable audio amplifier
Register E1h bit 0	0: NiMH battery 1: Li-ion battery
Register E1h bit 1	CPU thermal high

1.4.6 Processor

Table 1-12 Processor Specifications

Item	Specification
CPU type	P54CSLM-120,P54CSLM-133, P54CSLM-150, P55CLM-133, P55CLM - 150
CPU package	SPGA
Switchable processor speed (Y/N)	Yes
Minimum working speed	0MHz while hibernation mode
CPU voltage	3.1V/2.9V/2.45V

1.4.7 BIOS

Table 1-13 BIOS Specifications

Item	Specification
BIOS vendor	Acer
BIOS version	v2.1
BIOS in flash EPROM (Y/N)	Yes
BIOS ROM size	256KB
BIOS package type	32-pin TSOP
Same BIOS for STN color/TFT color (Y/N)	Yes

The BIOS can be overwritten/upgradeable using the "AFLASH" utility (AFLASH.EXE). Please refer to software specification section for details.

1.4.8 System Memory

Memory is upgradeable from 8 to 64 MB, employing 8-/16-/32-MB 64-bit soDIMMs (Small Outline Dual Inline Memory Modules). After installing the memory modules, the system automatically detects and reconfigures the total memory size during the POST routines. The following lists important memory specifications.

- Memory bus width: 64-bit
- Expansion RAM module type:144-pin, 64-bit, small outline Dual Inline Memory Module (soDIMM)
- Expansion RAM module size/configuration:
  - 8MB (1M*16 x4)
  - 16MB (2M*8 x8)
  - 32MB (4M*16 x4)
- Expansion RAM module speed/voltage/package: 60ns/3.3v/TSOP EDO
- EDO and fast-page mode DIMMs may be used together in a memory configuration.

The following table lists all possible memory configurations.
Table 1-14 Memory Configurations

Slot 1	Slot 2	Total Memory
8 MB	0 MB	8 MB
0 MB	8 MB	8 MB
8 MB	8 MB	16 MB
16 MB	0 MB	16 MB
0 MB	16 MB	16 MB
16 MB	8 MB	24 MB
8 MB	16 MB	24 MB
16 MB	16 MB	32 MB
32 MB	0 MB	32 MB
0 MB	32 MB	32 MB
32 MB	8 MB	40 MB
8 MB	32 MB	40 MB
32 MB	16 MB	48 MB
16 MB	32 MB	48 MB
32 MB	32 MB	64 MB

1.4.9 Second-Level Cache

This notebook supports 256KB pipeline burst second-level (L2) cache.

1.4.10 Video Memory

Table 1-15 Video RAM Configuration

Item	Specification
DRAM or VRAM	DRAM(EDO type)
Fixed or upgradeable	Fixed
Memory size/configuration	1MB (256K x 16 x 2pcs)
Memory speed	60ns
Memory voltage	3.3V
Memory package	TSOP

1.4.11 Video

Table 1-16 Video Hardware Specification

Item	Specification
Video chip	C&T65550B
Working voltage	C&T65550B: 3.3V C&T65550XX: 3.3V/5V ("XX" represents codes other than "A" (i.e. "B1"))
Video Chip substitutability	Yes During power-on, system supplies 5V to video chip and read its register to determine whether the video chip is 5V or 3.3V/5V type. If 5V video chip is detected, system maintains video voltage at 5V; if 3.3V/5V video chip is detected, system switches video voltage to 3.3V.

1.4.11.1 External CRT Resolution Support

Table 1-17 Supported External CRT Resolutions

Resolution x Color on External CRT	CRT Refresh Rate		Simultaneous on TFT LCD	Simultaneous on STN LCD
	CRT only	Simultaneous	SVGA	SVGA
640x480x16	60,75,85	60	Y	Y
640x480x256	60,75,85	60	Y	Y
640x480x65,536	60,75,85	60	Y	Y
640x480x16,777,216	60,75,85	60	Y	N
800x600x16	56,60,75	60	Y	Y
800x600x256	56,60,75	60	Y	Y
800x600x65,536	56,60	60	Y	N
1024x768x16	60,75,86I	60	Y	Y

Table 1-17 Supported External CRT Resolutions (Continued)

Resolution x Color on External CRT	CRT Refresh Rate		Simultaneous on TFT LCD	Simultaneous on STN LCD
1024x768x256	60,75,86I	60	Y	Y

1280x1024x16	86I	60	Y	Y

1.4.11.2 LCD Resolution Support

Table 1-18 Supported LCD Resolutions

Resolution x Color on LCD Only	TFT LCD (SVGA)	STN LCD (SVGA)
640x480x16	Y	Y
640x480x256	Y	Y
640x480x65,536	Y	Y
640x480x16,777,216	Y	-
800x600x16	Y	Y
800x600x256	Y	Y
800x600x65,536	Y	-
1024x768x16	Y	Y
1024x768x256	Y	Y

- DSTN color number: 256 colors
- TFT color number: 65536 colors
- Maximum resolution (LCD Panel): 800x600
- Maximum resolution (External CRT): 1280x1024

Using software, you can set the LCD to a higher resolution than its physical resolution, but the image shown on the LCD will pan.

1.4.12 Parallel Port

Table 1-19 Parallel Port Configurations

Item	Specification
Number of parallel ports	1
ECP/EPP support	Yes (set by BIOS setup)
Connector type	25-pin D-type
Location	Rear side
Selectable parallel port (by BIOS Setup)	• Parallel 1 (3BCh, IRQ7) • Parallel 2 (378h, IRQ7) • Parallel 3 (278h, IRQ5) • Disable

1.4.13 Serial Port

Table 1-20 Serial Port Configurations

Item	Specification
Number of serial ports	1
16550 UART support	Yes
Connector type	9-pin D-type
Location	Rear side
Selectable serial port (by BIOS Setup)	• Serial 1 (3F8h, IRQ4) • Serial 2 (2F8h, IRQ3) • Disable

1.4.14 Audio

Table 1-21 Audio Specifications

Item	Specification
Chipset	YMF715
Audio onboard or optional	Built-in
Mono or stereo	Stereo
Resolution	16-bit
Compatibility	SB-16 , Windows Sound System
Mixed sound sources	Voice, Synthesizer, Line-in, Microphone, CD
Voice channel	8-/16-bit, mono/stereo
Sampling rate	44.1 kHz
Internal microphone	No
Internal speaker / quantity	Yes / 2 pcs.
Microphone jack	Yes
Headphone jack	Yes

1.4.15 PCMCIA

PCMCIA is an acronym for Personal Computer Memory Card International Association. The PCMCIA committee set out to standardize a way to add credit-card size peripheral devices to a wide range of personal computers with as little effort as possible.

There are two type II/I or one type III PC Card slots found on the left panel of the notebook. These slots accept credit-card-sized cards that enhances the usability and expandability of the notebook.

ZV (Zoomed Video) port support allows your system to support hardware MPEG in the form of a ZV PC card.

Table 1-22 PCMCIA Specifications

Item	Specification
Chipset	TI 1131
Supported card type	Type-II / Type-III
Number of slots	Two Type-II or one Type-III
Access location	Left side
ZV (Zoomed Video) port support	Yes (only in lower slot)

1.4.16 Touchpad

Table 1-23 Touchpad Specifications

Item	Specification
Vendor & model name	Synaptics TM1002MPU
Power supply voltage (V)	5 ± 10%
Location	Palm-rest center
Internal & external pointing device work simultaneously	Yes
Support external pointing device hot plug	Yes
X/Y position resolution (points/mm)	20
Interface	PS/2 (compatible with Microsoft mouse driver)

1.4.17 Keyboard

Table 1-24 Keyboard Specifications

Item	Specification
Vendor & model name	SMK KAS1901-0161R (English)
Total number of keypads	84/85 keys
Windows 95 keys	Yes, (Logo key / Application key):
Internal & external keyboard work simultaneously	Yes

1.4.17.1 Windows 95 Keys

The keyboard has two keys that perform Windows 95-specific functions. See Table 1-26.

Table 1-25 Windows 95 Key Descriptions

Key	Description
Windows logo key	Start button. Combinations with this key performs special functions. Below are a few examples: • *Windows* + *Tab* Activate next Taskbar button • *Windows* + *E* Explore My Computer • *Windows* + *F* Find Document • *Windows* + *M* Minimize All • *Shift* + *Windows* + *M* Undo Minimize All • *Windows* + *R* Display Run dialog box
Application key	Opens the application's context menu (same as right-click).

1.4.18 FDD

Table 1-26 FDD Specifications

Item	Specification		
Vendor & model name	Mitsumi D353F2		
Floppy Disk Specifications			
Media recognition	2DD (720K)	2HD (1.2M, 3-mode)	2HD (1.44M)
Sectors / track	9	15	18
Tracks	80	80	80
Data transfer rate (Kbits/s)	250 300	500	500
Rotational speed (RPM)	300 360	360	300
Read/write heads	2		
Encoding method	MFM		
Power Requirement			
Input Voltage (V)	+5 ± 10%		

1.4.19 HDD

Table 1-27 HDD Specifications

Item	Specification			
Vendor & Model Name	IBM DMCA21080	IBM DMCA21440	IBM DTNA22160	Toshiba MK1002MAV
Drive Format				
Capacity (MB)	1080	1440	2160	1085
Bytes per sector	512	512	512	512
Logical heads	16	16	16	16
Logical sectors	63	63	63	63
Logical cylinders	2100	2800	4200	2100
Physical read/write heads	3	4	6	6
Disks	2	2	3	3
Spindle speed (RPM)	4009	4009	4000	4635
Performance Specifications				
Buffer size (KB)	128	96	96	128
Interface	ATA-3	ATA-3	ATA-3	ATA-3
Data transfer rate (disk-buffer, Mbytes/s)	39.5 ~ 61.8	39.5 ~ 61.8	39.1~ 61.6	29.3 ~ 55.5

Item	Specification			
Performance Specifications				
Data transfer rate (host-buffer, Mbytes/s)	16.6 (max., PIO mode 4)	16.6 (max., PIO mode 4)	16.6 (max., PIO mode 4)	16.6 (max., PIO mode 4)
DC Power Requirements				
Voltage tolerance (V)	5 ± 5%	5 + 5%, -10%	5 ± 5%	5 ± 5%

1.4.20 CD-ROM

Table 1-28 CD-ROM Specifications

Item	Specification
Vendor & Model Name	Panasonic UJDCD8730
Performance Specification	
Speed (KB/sec)	150 (normal speed) 1500 (10X speed)
Access time (ms)	170 (Typ.)
Buffer memory (KB)	128
Interface	Enhanced IDE (ATAPI) compatible
Applicable disc format	CD-DA, CD-ROM, CD-ROM XA (except ADPCM), CD-I, Photo CD (Multisession), Video CD, CD+
Loading mechanism	Drawer type, manual load/release
Power Requirement	
Input Voltage (V)	5

1.4.21 Battery

Table 1-29 Battery Specifications

Item	Specification		
Battery gauge on screen	Yes, by hotkey	Yes, by hotkey	Yes, by hotkey
Vendor & model name	Sanyo BTP-W31	Sony BTP-T31	Toshiba BTP-X31
Battery type	NiMH	Li-Ion	NiMH
Cell capacity (mAH)	3500	4050	3500
Cell voltage (V)	1.2	3.6	1.2
Number of battery cell	9-cell	9-Cell	9-Cell
Package configuration	9 serial	3 serial, 3 parallel	9 serial
Package voltage (V)	10.8	10.8	10.8
Package capacity (WAH)	37.8	40.5	37.8

1.4.22 Charger

To charge the battery, place the battery pack inside the battery compartment and plug the AC adapter into the notebook and an electrical outlet. The adapter has three charging modes:

- Rapid mode

  The notebook uses rapid charging when power is turned off and a powered AC adapter is connected to it. In rapid mode, a fully depleted battery gets fully charged in approximately two hours.

- Charge-in-use mode

  When the notebook is in use with the AC adapter plugged in, the notebook also charges the battery pack if installed. This mode will take longer to fully charge a battery than rapid mode. In charge-in-use mode, a fully depleted battery gets fully charged in approximately six to eight hours.

- Trickle mode

  When the battery is fully charged, the adapter changes to trickle mode to maintain the battery charge level. This prevents the battery from draining while the notebook is in use.

Table 1-30 Charger Specifications

Item	Specification
Vendor & model name	Ambit T62.062.C.00
Input voltage (from adapter, V)	19 (min.) 20 (typ.), 20.5 (max.)
Battery Low Voltage	
Battery Low 1 level (V)	10.7 (typ., for NiMH) 8.65 (typ., for LIB)
Battery Low 2 level (V)	10.35 (typ., for NiMH) 8.23 (typ., for LIB)
Battery Low 3 level (V)	9.22 (typ., for NiMH) 7.73 (typ., for LIB)
Charge Current	
Fast charge (charge when system is still operative, A)	0.65 (typ.)
Quick charge (charge while system is not operative, A)	1.9 (typ.)
Charging Protection	
Safety timer for Fast Charge mode while notebook is operating (minute)	576 (NiMH)
Safety timer for Quick Charge mode while notebook is not operating (minute)	192 (NiMH)
Maximum temperature protection (ºC)	60
Maximum voltage protection (V)	16.2V for NiMH
Over voltage protection	13V for Li-ion

1.4.23 DC-DC Converter

DC-DC converter generates multiple DC voltage level for whole system unit use.

Table 1-31 DC-DC Converter Specifications

Item	Specification					
Vendor & model name	Ambit T62.061.C.00					
Input voltage (Vdc)	8~21					
Output Rating	**5V**	**3.3V**	**2.9V (2.35/2.45/2.9/3.1V)**	**+12V**	**+6V**	**5VSB**
Current (w/ load, A)	0~3.2	0~3.3	0~3.0	0~0.15	0~0.1	0.005
Voltage ripple (max., mV)	75	75	50	100	300	75
Voltage noise (max., mV)	100	100	100	200	500	100
OVP (Over Voltage Protection, V)	6.5~8.2	4.5~6.2	3.3~5.0 for 2.9/3.1/2.35V/2.45V	14~20	7~9	-

1.4.24 DC-AC Inverter

DC-AC inverter is used to generate very high AC voltage, then supply to LCD CCFT backlight use, and is also responsible for the control of LCD brightness. Avoid touching the DC-AC inverter area while the system unit is turned on.

Table 1-32 DC-AC Inverter Specifications

Item	Specification		
Vendor & model name	Ambit T62.066.C.00 / Ambit T62.064.C.00		
Input voltage (V)	7.3 (min.)	-	20 (max.)
Input current (mA)	-	420 (typ.)	550 (max.)
Output voltage (Vrms, no load)	1000 (min.)	-	1500 (max.)
Output voltage frequency (kHz)	25 (min.)	42 (typ.)	60 (max.)
Output current (mArms)	1.5~5.5 (min.)	2.0~6.0 (typ.)	2.5~6.5 (max.)

1.4.25 LCD

Table 1-33 LCD Specifications

Item	Specification			
Vendor & model name	HITACHI LMG9900ZWCC	TORiSAN LM-FH53-22NAW	IBM ITSV45E	GOLDSTAR LP121S1-J
Mechanical Specifications				
LCD display area (diagonal, inch)	11.3	11.3	11.3	12.1
Display technology	STN	STN	TFT	TFT
Resolution	SVGA (800x600)	VGA (800x600)	SVGA (800x600)	SVGA (800x600)
Supported colors	--	--	262,144 colors	262,144 colors
Optical Specification				
Contrast ratio	30 (typ.)	30 (typ.)	100 (typ.)	100 (typ.)
Brightness (cd/m^2)	70 (typ.)	70 (typ.)	70 (typ.)	70 (typ.)
Brightness control	keyboard hotkey	keyboard hotkey	keyboard hotkey	keyboard hotkey
Contrast control	using keyboard hotkey	using keyboard hotkey	none	none
Electrical Specification				
Supply voltage for LCD display	3.3 or 5 (typ.)	3.3 (typ.)	3.3	3.3 (typ.), 3.63 (max.)
Supply voltage for LCD backlight (Vrms)	590 (typ.)	590 (typ.)	590	480

The LCD ID code can be set by using the LCD ID utilization utility (370pw.exe/370pr.exe). Please refer to the software specification section for details.

1.4.26 AC Adapter

Table 1-34 AC Adapter Specifications

Item	Specification
Vendor & model name	Delta ADP-45GB REV.E2
Input Requirements	
Nominal voltages (Vrms)	90 - 264
Frequency variation range (Hz)	47 - 63
Maximum input current (A, @90Vac, full load)	1.5 A
Inrush current	The maximum inrush current will be less than 50A and 100A when the adapter is connected to 115Vac(60Hz) and 230Vac(50Hz) respectively.
Efficiency	It should provide an efficiency of 83% minimum, when measured at maximum load under 115V(60Hz)
Output Ratings (CV mode)	
DC output voltage (V)	+19
Noise + Ripple (mV)	300
Load (A)	0 (min.) 2.4 (max.)
Dynamic Output Characteristics	
Turn-on delay time (s, @115Vac)	2
Hold up time (ms; @115 Vac input, full load)	5 (min.)
Over Voltage Protection (OVP, V)	26
Short circuit protection	Output can be shorted without damage
Electrostatic discharge (ESD, kV)	±15 (at air discharge)
Dielectric Withstand Voltage	
Primary to secondary	3000 Vac (or 4242 Vdc), 10 mA for 1 second
Leakage current	0.25 mA maximum @ 254 Vac, 60Hz.
Regulatory Requirements	
Internal filter meets: 1. FCC class B requirements. 2. CISPR 22 Class B requirements.	

1.5 Software Configuration and Specification

1.5.1 BIOS

The BIOS is compliant to PCI v2.1, APM v1.2, E-IDE and PnP specification. It also defines the hotkey functions and controls the system power-saving flow.

1.5.1.1 Keyboard Hotkey Definition

The notebook supports the following hotkeys.

Table 1-35 Hotkey Descriptions

Hotkey	Icon	Function	Description
Fn-Esc		Hotkey Escape	Exits the hotkey control.
Fn-F1	?	Hotkey Help	Displays the hotkey list and help. Press | to exit the screen.
Fn-F2		Brightness Control  Contrast Control 	Toggles between brightness control and contrast control. Press the scale hotkeys (Fn- →and Fn -←) to increase and decrease the brightness or contrast level. Notebooks with TFT displays do not show the brightness control icon.
Fn-F3		Display Toggle	Switches display from LCD to CRT to both LCD and CRT.
Fn-F4		Battery Gauge 	Displays the battery gauge.
Fn-F5		Volume Control 	Press the scale hotkeys (Fn-→ and Fn-←) to increase and decrease the output level.
Fn-F6		Setup	Gains access to BIOS Setup's Advanced System Configuration parameters.
Fn-F7	Z^{Z}	Hibernation/Standby	Enters hibernation mode if the 0-volt suspend function is installed and enabled; otherwise, the notebook enters standby mode.
Fn-→		Scale Increase	Increases the setting of the current icon.
Fn-←		Scale Decrease	Decreases the setting of the current icon.
Fn-T		Toggle Touchpad	Turns the internal touchpad on and off.

When the available hotkey is toggled, the system will issue a beep to enter the assigned process.

1.5.1.2 MultiBoot

The system can boot from the FDD, External FDD, HDD, CD-ROM. The user can select the desired booting process to boot the system. If the CD-ROM is bootable, the BIOS will override the other process to boot the system directly.

1.5.1.3 Power Management

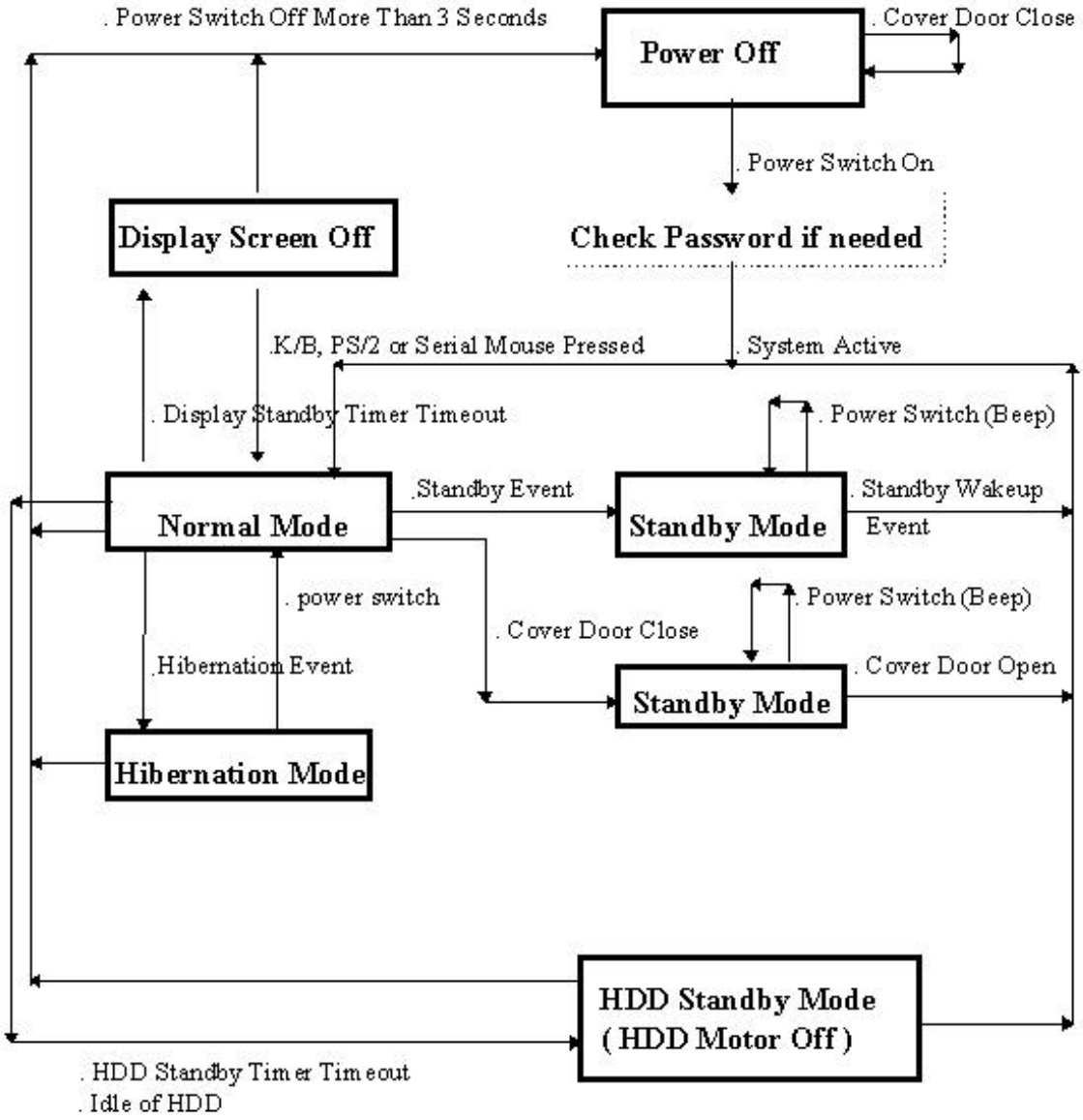


Figure 1-14 Power Management Block Diagram

ON MODE

Normal full-on operation

STANDBY MODE

The notebook consumes very low power in standby mode. Data remain intact in the system memory until battery is drained.

The necessary condition for the notebook to enter standby mode is that the reserved disk space size for saving system and video memory is insufficient so the notebook is unable to enter hibernation mode. In this situation, there are three ways to enter standby mode:

- Press the standby/hibernation hotkey Fn-F7 (Z^z)
- Set a value for the System Standby/Hibernation Timer in Setup. If the waiting time specified by this timer elapses without any system activity, the notebook goes into standby mode.
- Invoked by the operating system power saving modes

The following signals indicate that the notebook is in standby mode:

- The buzzer beeps (when you press the standby/hibernation hotkey)
- The indicator light flashes

To leave standby mode and return to normal mode, press the any key. If an incoming PCMCIA modem event occurs and the Modem Ring Wake Up From Standby is enabled, the system returns to normal mode.

Table 1-36 Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter Standby Mode	• "Hard Disk Drive" is [Disabled] in System Security of BIOS SETUP. • "Hard Disk 0" is [None] in Basic System Configuration of BIOS SETUP. • HDD has not located enough free contiguous disk space generated by Sleep Manager and this free space is not corrupted. • Standby/Hibernation Timer times-out or Standby/Hibernation HotKey pressed and there is no activity within 1/2 second.
The condition of Standby Mode	• Issue a beep. • Flash standby LED with 1 Hz frequency. • Disable the mouse, serial and the parallel port. • The keyboard controller, HDD and VGA enter the standby mode. • Stop the CPU internal clock. • All the functions are disabled except the keyboard, battery low warning and modem ring wake up from standby (if enabled).
The condition back to On Mode	Any one of following activities will let system back to Normal Mode: • Any keystroke (Internal KB or External KB) • Modem ring.

HIBERNATION MODE

In hibernation mode (also known as zero-volt hibernation-to-disk mode), power shuts off. The notebook saves all system information onto the hard disk before it enters hibernation mode. Once you turn on the power, the notebook restores this information and resumes where you left off upon leaving hibernation mode.

A necessary condition for the notebook to enter hibernation mode is that the reserved space for saving system information on the hard disk must be larger than the combined system and video memory size. Under such conditions, the standby/hibernation hotkey acts as the hibernation hotkey. See the user's manual for information on the Sleep Manager utility.
In this situation, there are four ways to enter hibernation mode:

- Press the standby/hibernation hotkey Fn-F7 (Z^z)
- Set a value for the System Standby/Hibernation Timer in Setup. If the waiting time specified by this time elapses without any system activity, the system goes into hibernation mode
- Enable the Suspend upon Battery-low parameter in Setup. If a battery-low condition takes place, the notebook enters hibernation mode in about five minutes.
- Invoked by the operating system power saving modes

When the notebook enters hibernation mode, the whole system does not consume any power. This is why hibernation mode is also called zero-volt suspend.
To exit hibernation mode, press the power switch (⏻).

When the PCMCIA I/O card is detected, the following warning pop-up message will be displayed on the screen by the BIOS. The system will wait for the specified key to continue.

Warning!!

A PCMCIA card is detected!!

If you are using a fax/modem or LAN cards, please disconnect with server or complete transmission before entering standby/hibernation mode, otherwise :

1) File server will be shut down if LAN card is used.

2) Data will be lost if a modem card is used.

Press <F1> to enter standby/hibernation mode.

Press <F2> to cancel.

Table 1-37 Hibernation Mode Conditions and Descriptions

Condition	Description
The condition to enter Hibernation Mode	• "Hard Disk Drive" is not [Disabled] in System Security of BIOS SETUP. • "Hard Disk 0" is not [None] in Basic System Configuration of BIOS SETUP. • HDD has already located enough free contiguous disk space generated by the Sleep Manager and this free space is not corrupted. • Standby/Hibernation Timer times-out or Standby/Hibernation Hotkey pressed and there is no activity within 1/2 second.
The condition of Hibernation Mode	• Except the RTC, 6375 (state machine), KB controller and power switch, all the system components are off.
The condition back to On Mode	• Turn off then on the system.

DISPLAY STANDBY MODE

Screen activity is determined by the keyboard, the built-in touchpad, and an external PS/2 pointing device. If these devices are idle for the period specified by the Display Standby Timer, the display shuts off until you press a key or move the touchpad or external mouse.

Table 1-38 Display Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter Display Standby Mode	• Pointing device is idle until Display Standby Timer times-out or LCD cover is closed.
The condition of Display Standby Mode	• All the system components are on except LCD backlight and CRT horizontal frequency output (if CRT is connected)
The condition back to On Mode	• Any keystroke (Internal KB or External KB) • Pointing device activity

The VGA BIOS should support DPMS (Desktop Power Management System) for the standby and hibernation mode function call. When the Display Standby Timer expires, the system BIOS will execute the DPMS service routines.

HARD DISK STANDBY MODE

The hard disk enters standby mode when there are no disk read/write operations within the period of time specified by the Hard Disk Standby Timer. In the standby state, the power supplied to the hard disk is reduced to a minimum. The hard disk returns to normal once the system accesses it.

Table 1-39 Hard Disk Standby Mode Conditions and Descriptions

Condition	Description
The condition to enter HDD Standby Mode	• Display Standby Timer times-out or LCD cover is closed.
The condition of HDD Standby Mode	• All the system components are on except HDD spindle motor
The condition back to On Mode	• Any access to HDD

BATTERY LOW

When the battery capacity is low and has no adapter plugged, the system will generate the following battery low warning:

- Flash power LED with 4 Hz.
- Issue 4 short beeps per minute (if enabled in setup).
- If the AC adapter does not plug in within 3 minutes and the "Standby/Hibernation upon Battery-low" in BIOS SETUP is enabled, the system will enter Standby/0-Volt Hibernation Mode. The battery low warning will stop as soon as the AC adapter is plugged into the system.

THE AUTODIM PROCESS OF THE LCD BRIGHTNESS

The notebook has a unique **"automatic dim"** power saving feature. When the notebook is using AC power and you disconnect the AC adapter from the notebook, the system "decides" whether or not to automatically dim the LCD backlight to save power.
If the LCD backlight is too bright, the system automatically adjusts it to a manageable level; otherwise, the level stays the same. If you want a brighter picture, you can then adjust the brightness and contrast level using hotkeys (Fn-F2).
If you reconnect AC power to the system, the system automatically adjusts the LCD backlight to its original level — the brightness and contrast level before disconnecting the AC adapter. If you adjusted the brightness and contrast level after disconnecting AC power, the level stays the same after you reconnect the AC adapter.
There are two reasons for the notebook to have the LCD AutoDim feature. The first is to save the power during the notebook is operating under the DC mode. The second is to save the "favorite" brightness parameter set by the user.
The following processes are the basic methods used to implement the LCD brightness AutoDim.

1. If the original brightness is over 75% and the AC power is on-line, the BIOS will change the brightness to 75% after the AC power is off-line.
2. If the original brightness is below 75%, the brightness maintains the same level even if the AC power is off-line.
3. If the brightness is already changed by the hotkey under DC power, it will not be changed after the AC power is plugged in.
4. If the brightness is not changed by the hotkey under DC power, the brightness will be changed back to the old setting — the previous brightness parameter under AC power.
5. If the previous brightness parameter does not exist, the brightness will not be changed in process 4.

1.5.2 Drivers, Applications and Utilities

The notebook comes preloaded with the following software:

- Windows 95[2]
- System utilities and application software[3]
  - Sleeper manager utility
  - Touchpad driver
  - Display drivers
  - Audio drivers
  - PC Card slot drivers and applications
  - Other third-party application software

Table 1-40 Location of Drivers in the System Utility CD

Device Category	Function	Location
Sound, video and game controllers	Audio	ENGLISH\WIN95\AUDIO\
Mouse	Mouse	ENGLISH\WIN95\MOUSE\
Display adapters	Video	ENGLISH\WIN95\VGA\
PCMCIA	Zoomed Video Port	English\Win95\PCMCIA\

To re-install applications under Windows 95, click on Start, then Run…. Based on the location of the application, run the setup program to install the application. The following table lists the applications and their locations:

Table 1-41 Location of Applications in the System Utility CD

Name	Function	Location
Sleep Manager	0V Suspend utility	ENGLISH\WIN95\SLEEPMGR\
Y-Station	Audio application	ENGLISH\WIN95\Ystation
SafeOFF	Protect if user accidentally press the power switch	ENGLISH\WIN95\SAFEOFF

Drivers for Windows 3.x and Windows NT are also found in the System Utility CD if you should need them.

2 In some areas, a different operating system may be pre-loaded instead of Windows 95.

3 The system utilities and application software list may vary.

1.6 System Block Diagram

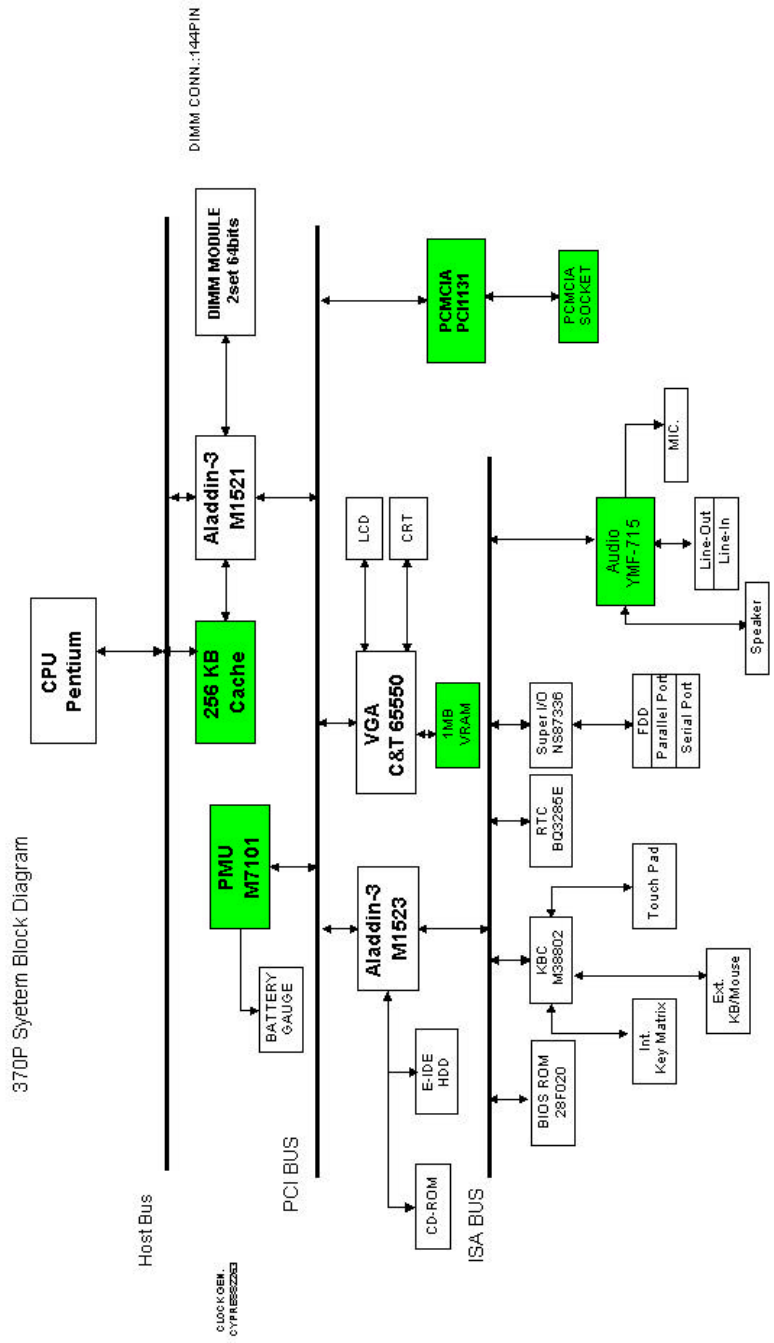


Figure 1-15 System Block Diagram

1.7 Environmental Requirements

Table 1-42 Environmental Requirements

Item	Specification
Temperature	
Operating (ºC)	+5°C ~ +35°C
Non-operating(ºC)	-20°C ~ +60°C
Humidity	
Operating (non-condensing)	20% ~ 80%
Non-operating (non-condensing)	20% ~ 80%
Operating Vibration (unpacked)	
Operating	5 - 25.6Hz, 0.38mm; 25.6 - 250Hz, 0.5G
Sweep rate	> 1 minute / octave
Number of test cycles	2 / axis (X,Y,Z)
Non-operating Vibration (unpacked)	
Non-operating	5 - 27.1Hz, 0.6G; 27.1 - 50Hz, 0.41mm; 50~500Hz, 2G
Sweep rate	> 2 minutes / octave
Number of text cycles	4 / axis (X,Y,Z)
Shock	
Non-operating (unpacked)	40G peak, 11±1ms, half-sine
Non-operating (packed)	50G peak, 11±1ms, half-sine
Altitude	
Operating	10,000 feet
Non-operating	40,000 feet
ESD	
Air discharge	8kV (no error) 12.5kV (no restart error) 15kV (no damage)
Contact discharge	4kV (no error) 6kV (no restart error) 8kV (no damage)

1.8 Mechanical Specifications

Table 1-43 Mechanical Specifications

Item	Specification
Weight FDD model CD-ROM model	(includes battery) 2.6 kg. (5.7 lb.) 2.8 kg. (6.2 lb.)
Dimensions (main footprint)	W x D x H 306mm x 228mm x 46mm (12.05” x 8.98” x 1.81”)

Major Chips Description

This chapter discusses the major chips used in the notebook.

2.1 Major Component List

Table 2-1 Major Chips List

Component	Vendor	Description
M1521	Acer	System data buffer
M1523	Acer	System controller chip
M7101	Acer	Power management unit
65550	C&T (Chips & Technology)	Video controller
TI PCI1131	Texas Instrument	PCMCIA controller
NS87336VJG	NS (National Semiconductor)	Super I/O controller
YMF715	Yamaha	Audio Chip
T62.062.C	Ambit	Battery Charger
T62.061.C	Ambit	DC-DC Converter
T62.064.C	Ambit	DC-AC Inverter for 11.3”
T62.066.C	Ambit	DC-AC Inverter for 12.1”

2.2 ALI M1521

The ALADDIN-III consists of two chips, ALI M1521 and M1523 to give a 586 class system the complete solution with the most up-to-date feature and architecture for the new multimedia/multithreading operating system. It utilizes the BGA package to improve the AC characterization, resolves system bottleneck and make the system manufacturing easier. The ALADDIN-III gives a highly-integrated system solution and a most up-to-date system architecture including the UMA, ECC, PBSRAM, SDRAM/BEDO, and multi-bus with highly efficient, deep FIFO between the buses, such as the HOST/PCI/ISA dedicated IDE bus.

The M1521 provides a complete integrated solution for the system controller and data path components in a Pentium-based system. It provides 64-bit CPU bus interface, 32-bit PCI bus interface, 64/72 DRAM data bus with ECC or parity, secondary cache interface including pipeline burst SRAM or asynchronous SRAM, PCI master to DRAM interface, four PCI master arbiters, and a UMA arbiter. The M1521 bus interfaces are designed to interface with 3V and 5V buses. It directly connects to 3V CPU bus, 3V or 5V tag, 3V or 5V DRAM bus, and 5V PCI bus.

2.2.1 Features

- Supports all Intel/Cyrix/AMD 586-class processors (with host bus of 66 MHz, 60 MHz and 50 MHz at 3V)
  - supports M1/K5/Dakota CPUs
  - supports linear wrap mode for M1
- Supports asynchronous/pipeline-burst SRAM
  - Write-back/dynamic write-back cache policy
  - Built-in 8K*2 bit SRAM for MESI protocol to cost and enhance performance
  - Cacheable memory up to 512MB with 11-bit tag SRAM
  - Supports 3V/5V SRAMs for tag address
- Supports FPM/EDO/BEDO/SDRAM DRAMs
  - RAS lines
  - 64-bit data path to memory
  - Symmetrical/asymmetrical DRAMs
  - 3V or 5V DRAMs
  - Duplicated MA[1:0] driving pins for burst access
  - No buffer needed for RASJ and CASJ and MA[1:0]
  - CBR and RAS-only refresh
  - Supports 64M-bit (16M*4, 8M*8, 4M*16) technology DRAMs
  - Supports programmable-strength MA buffer
  - Supports error checking and correction (ECC) and parity for DRAM
  - Supports the most flexible six 32-bit populated banks of DRAM (to spare 12MB for Windows 95)
  - Supports SIMM and DIMM

- UMA (unified memory architecture)
  - Dedicated UMA arbiter pins
  - Supports several protocols from major graphics vendors
  - SFB size : 512KB/1MB/2MB/3MB/4MB
  - CPU could access frame buffer memory through system memory controller
  - Alias address for frame buffer memory
- Fully synchronous 25/30/33 MHz 5V PCI interface
  - PCI bus arbiter: five PCI masters and M1523 supported
  - Dwords for CPU-to-PCI Memory write posted buffers
  - Convert back-to-back CPU to PCI memory write to PCI burst cycle
  - DWORDS for PCI-to-DRAM write-posted/read-prefetching buffers
  - PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write-back)
  - L1/L2 pipelined snoop ahead for PCI-to-DRAM cycle
  - Supports PCI mechanism #1 only
  - PCI spec. 2.1 support. [N(16/8)+8 rule, passive release, fair arbitration]
  - Enhanced performance for memory-read-line, memory-read-multiple, and memory-write-multiple
  - Invalidates PCI commands
- DRAM refresh during 5V system suspend
- I/O leakage stopper for power saving during system suspend
- 328-pin or 388-pin BGA process

2.2.2 Block Diagram

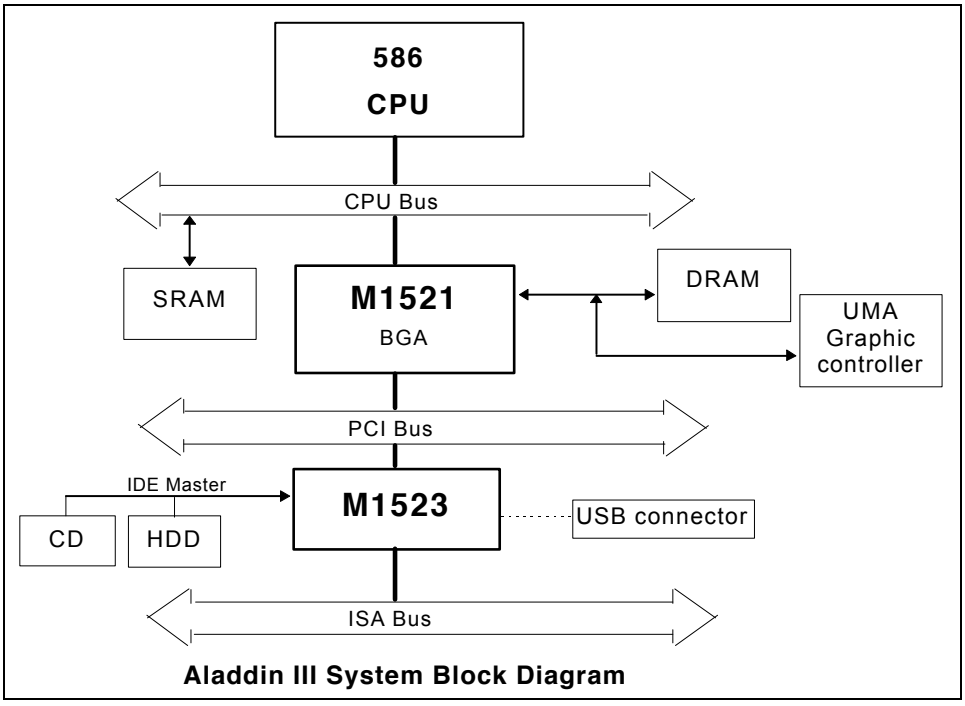


Figure 2-1 Alladin III Block Diagram

2.2.3 System Architecture

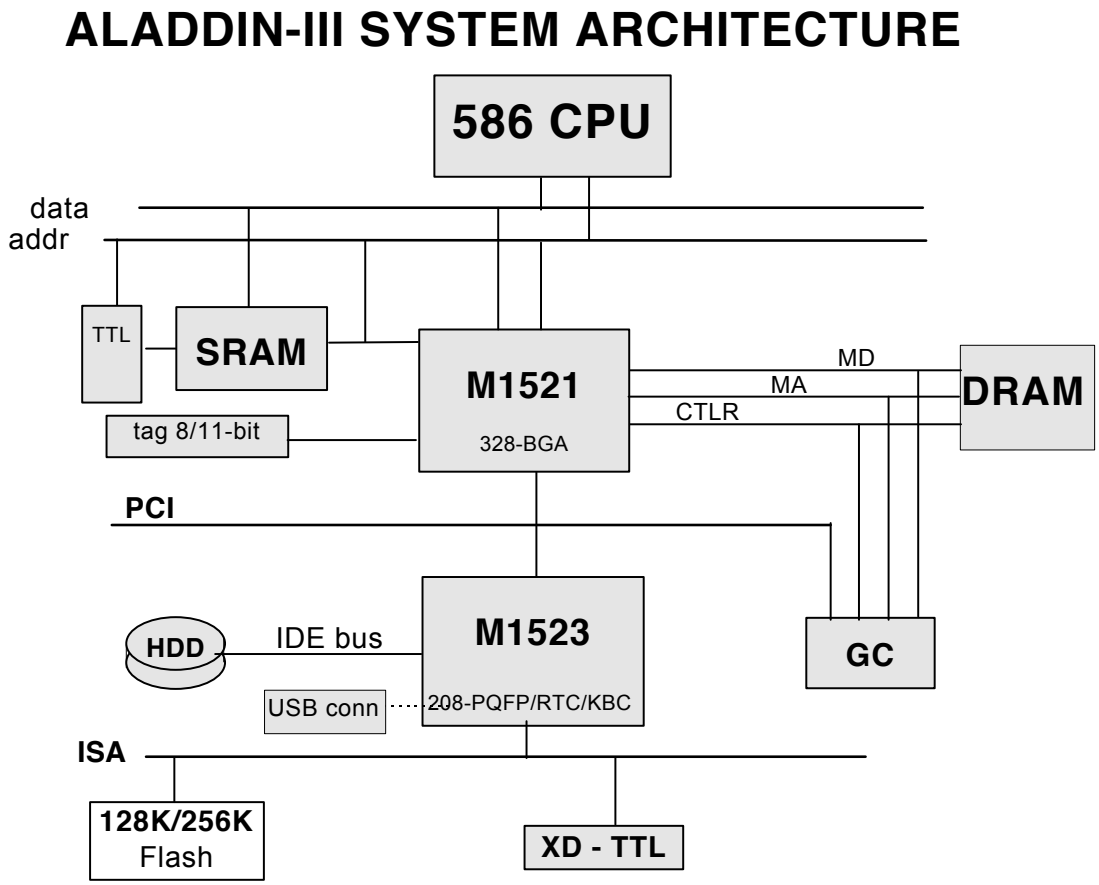


Figure 2-2 Alladin III System Architecture

2.2.4 Data Path

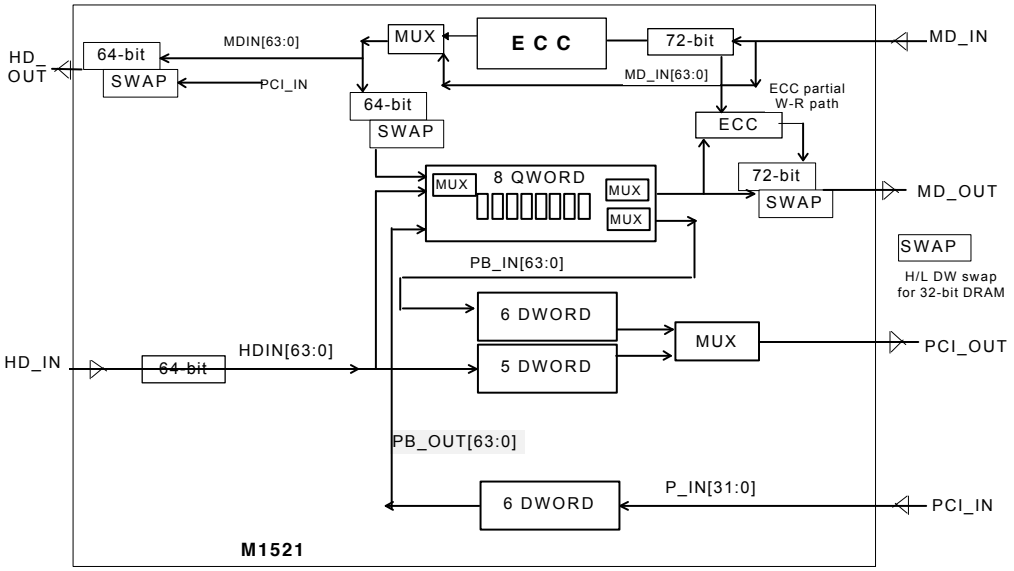
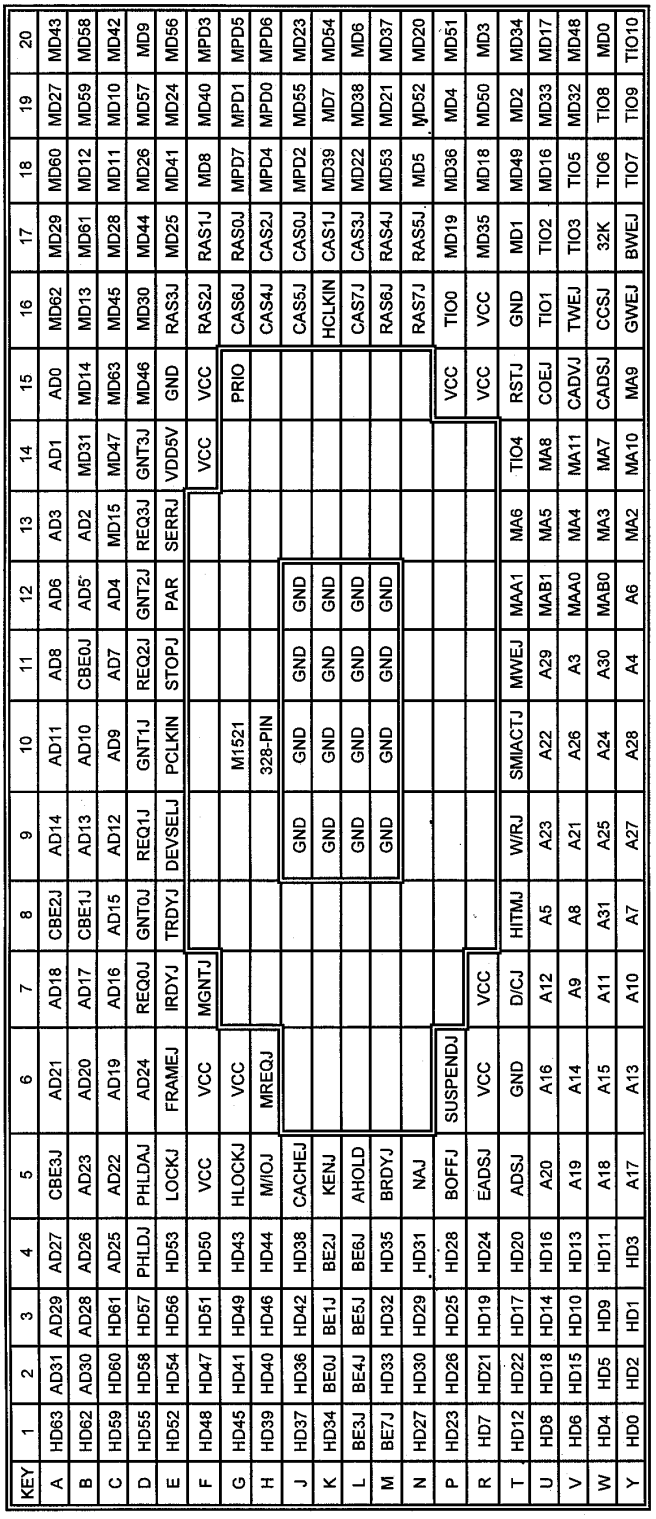


Figure 2-3 M1521 Data Path

2.2.5 Pin Diagram



KEY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD63	AD31	AD29	AD27	CBE3J	AD21	AD18	CBE2J	AD14	AD11	AD8	AD6	AD3	AD1	AD0	MD62	MD29	MD60	MD27	MD43
B	HD62	AD30	AD28	AD26	AD23	AD20	AD17	CBE1J	AD13	AD10	CBE0J	AD5	AD2	MD31	MD14	MD13	MD61	MD12	MD59	MD58
C	HD59	HD60	HD61	AD25	AD22	AD19	AD16	AD15	AD12	AD9	AD7	AD4	MD15	MD47	MD63	MD45	MD28	MD11	MD10	MD42
D	HD55	HD58	HD57	PHLDJ	PHLDAJ	AD24	REQ0J	GNT0J	REQ1J	GNT1J	REQ2J	GNT2J	REQ3J	GNT3J	MD46	MD30	MD44	MD26	MD57	MD9
E	HD52	HD54	HD56	HD53	LOCKJ	FRAMEJ	IRDYJ	TRDYJ	DEVSELJ	PCLKIN	STOPJ	PAR	SERRJ	VDD5V	GND	RAS3J	MD25	MD41	MD24	MD56
F	HD48	HD47	HD51	HD50	VCC	VCC	MGNTJ							VCC	VCC	RAS2J	RAS1J	MD8	MD40	MPD3
G	HD45	HD41	HD49	HD43	HLOCKJ	VCC				M1521					PRIO	CAS6J	RAS0J	MPD7	MPD1	MPD5
H	HD39	HD40	HD46	HD44	M/IOJ	MREQJ				328-PIN						CAS4J	CAS2J	MPD4	MPD0	MPD6
J	HD37	HD36	HD42	HD38	CACHEJ				GND	GND	GND	GND				CAS5J	CAS0J	MPD2	MD55	MD23
K	HD34	BE0J	BE1J	BE2J	KENJ				GND	GND	GND	GND				HCLKIN	CAS1J	MD39	MD7	MD54
L	BE3J	BE4J	BE5J	BE6J	AHOLD				GND	GND	GND	GND				CAS7J	CAS3J	MD22	MD38	MD6
M	BE7J	HD33	HD32	HD35	BRDYJ				GND	GND	GND	GND				RAS6J	RAS4J	MD53	MD21	MD37
N	HD27	HD30	HD29	HD31	NAJ											RAS7J	RAS5J	MD5	MD52	MD20
P	HD23	HD26	HD25	HD28	BOFFJ	SUSPENDJ									VCC	TIO0	MD19	MD36	MD4	MD51
R	HD7	HD21	HD19	HD24	EADSJ	VCC	VCC								VCC	VCC	MD35	MD18	MD50	MD3
T	HD12	HD22	HD17	HD20	ADSJ	GND	D/CJ	HITMJ	W/RJ	SMIACTJ	MWEJ	MAA1	MA6	TIO4	RSTJ	GND	MD1	MD49	MD2	MD34
U	HD8	HD18	HD14	HD16	A20	A16	A12	A5	A23	A22	A29	MAB1	MA5	MA8	COEJ	TIO1	TIO2	MD16	MD33	MD17
V	HD6	HD15	HD10	HD13	A19	A14	A9	A8	A21	A26	A3	MAA0	MA4	MA11	CADVJ	TWEJ	TIO3	TIO5	MD32	MD48
W	HD4	HD5	HD9	HD11	A18	A15	A11	A31	A25	A24	A30	MAB0	MA3	MA7	CADSJ	CCSJ	32K	TIO6	TIO8	MD0
Y	HD0	HD2	HD1	HD3	A17	A13	A10	A7	A27	A28	A4	A6	MA2	MA10	MA9	GWEJ	BWEJ	TIO7	TIO9	TIO10

Figure 2-4 M1521 Pin Diagram

2.2.6 Signal Descriptions

Table 2-2 M1521 Signal Descriptions

Signal	Pin	Type	Description
Host Interface			
A[31:29] A[28:26] A[25:23] A[22:20] A[19:17] A[16:14] A[13:11] A[10:08] A[07:05] A[04:03]	W8, W11, U11, Y10, Y9, V10, W9, W10, U9, U10, V9, U5, V5, W5, Y5, U6, W6, V6, Y6, U7, W7, Y7, V7, V8, Y8, Y12, U8, Y11, V11	I/O	Host Address Bus Lines. A[31:3] have two functions. As inputs, along with the byte enable signals, these serve as the address lines of the host address bus that defines the physical area of memory or I/O being accessed. As outputs, the M1521 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	M1, L4, L3, L2, L1, K4, K3, K2	I	Byte Enables. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these are ignored by the M1521.
ADSJ	T5	I	Address Strobe. The CPU or M1521 starts a new cycle by asserting ADSJ first. The M1521 does not precede to execute a cycle until it detects ADSJ active.
BRDYJ	M5	O	Burst Ready. The assertion of BRDYJ means the current transaction is complete. The CPU terminates the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	N5	O	Next Address. It is asserted by the M1521 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	L5	O	CPU A-Hold Request Output. It serves as the input of CPU's AHOLD pin and actively driven for inquiry cycles.
EADSJ	R5	O	External Address Strobe. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1521 asserts this signal to proceed snooping.
BOFFJ	P5	O	CPU Back-Off. If BOFFJ is sampled active, CPU floats all its buses in the next clock.
HITMJ	T8	I	Host Cache Hit after Modified. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written-back.

Table 2-2 M1521 Signal Descriptions (continued)

Signal	Pin	Type	Description
Host Interface			
M/IOJ	H5	I	Host Memory or I/O. This bus definition pin indicates the current bus cycle is either memory or input/ output.
D/CJ	T7	I	Host Data or Code. This bus definition pin is used to distinguish data access cycles from code access cycles.
W/RJ	T9	I	Host Write or Read. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	G5	I	Host Lock. When HLOCKJ is asserted by the CPU, the M1521 recognizes that the CPU is locking the current cycles.
CACHEJ	J5	I	Host Cacheable. This pin is used to indicate the host's internal cacheability of the read cycles. If it is driven inactive, the CPU does not cache the returned data regardless of the state of KENJ.
KENJ/INV	K5	O	Cache Enable Output. This signal connects to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1521 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	T10	I	SMM Interrupt Active. It is asserted by the CPU to inform the M1521 that SMM mode is being entered.
HD[63:0]	A1, B1, C3, C2, C1, D2, D3, E3, D1, E2, E4, E1, F3, F4, G3, F1, F2, H3, G1, H4, G4, J3, G2, H2, H1, J4, J1, J2, M4, K1, M2, M3, N4, N2, N3, P4, N1, P2, P3, R4, P1, T2, R2, T4, R3, U2, T3, U4, V2, U3, V4, T1, W4, V3, W3, U1, R1, V1, W2, W1, Y4, Y2, Y3, Y1	I/O	Host Data Bus Lines. These signals connect to the CPU's data bus.
DRAM Interface			
MPD[7:0]	G18, H20, G20, H18, F20, J18, G19, H19	I/O	DRAM Parity/ECC check bits. These are the 8-bit parity/ECC check bits over DRAM bus.
RASJ[7] / SRASJ[0]	N16	O	Row Address Strobe 7 or Synchronous DRAM RAS 0. FPM/EDO/BEDO of DRAM bank 7. SDRAM row address strobe (SDRAM) copy 0.

Table 2-2 M1521 Signal Descriptions (continued)

Signal	Pin	Type	Description
DRAM Interface			
RASJ[6] / SCASJ[0]	M16	O	Row Address Strobe 6, or Synchronous DRAM CAS 0 (FPM/EDO/BEDO) of DRAM bank 6. SDRAM column address strobe (SDRAM) copy 0.
RASJ[5:0] / SCSJ[5:0]	N17, M17, E16, F16, F17, G17	I/O	Row Address Strobes or synchronous DRAM chip select. These signals drives the corresponding RASJs of DRAMs or synchronous DRAM chip select[5:0].
CASJ[7:0] / DQM[7:0]	L16, G16, J16, H16, L17, H17, K17, J17	O	Column Address Strobes or Synchronous DRAM Input/Output Data Mask. These CAS signals should connect to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all the CASJs are active. In SDRAM, these pins act as synchronized output enables during a read cycle and a byte mask during a write cycle.
MA[11:2]	V14, Y14, Y15, U14, W14, T13, U13, V13, W13, Y13	O	DRAM Address lines. These signals are the address lines of all DRAMs. The M1521 supports DRAM types ranging from 256K to 64M.
MAA[1:0]	T12, V12	O	Memory Address copy A for [1:0]
MAB[1:0]	U12, W12	O	Memory Address copy B for [1:0]
MD[63:0]	C15, A16, B17, A18, B19, B20, D19, E20, J19, K20, M18, N19, P20, R19, T18, V20, C14, D15, C16, D17, A20, C20, E18, F19, K18, L19, M20, P18, R17, T20, U19, V19, B14, D16, A17, C17, A19, D18, E17, E19, J20, L18, M19, N20, P17, R18, U20, U18, C13, B15, B16, B18, C18, C19, C20, F18, K19, L20, N18, P19, R20, T19, T17, W20	I/O	Memory Data. These pins connect to DRAMs.
MWEJ[0]	T11	O	DRAM Write Enable. This is the DRAM write enable pin and behaves according to the early-write mechanism; i.e. it activates before the CASJs do. For refresh cycles, it remains deasserted.
Secondary Cache Interface			
CADVJ/CA4	V15	O	Synchronous SRAM advance or Asynchronous SRAM address line 4.
CADSJ/CA3	W15	O	Synchronous SRAM address strobe cache or Asynchronous SRAM address line 3.

Table 2-2 M1521 Signal Descriptions (continued)

Signal	Pin	Type	Description
Secondary Cache Interface			
CCSJ/CB4	W16	O	Synchronous SRAM chip select or Cache Address line 4 copy. This pin has two modes of operation depending on the type of SRAM selected via hardware strapping options or programming the CC register.
GWEJ	Y16	O	Synchronous SRAM Global Write Enable or Asynchronous SRAM Write Enable.
COEJ	U15	O	Synchronous/Asynchronous SRAM Output Enable.
BWEJ/CGCSJ	Y17	O	Synchronous SRAM Byte-Write Enable/ Asynchronous SRAM Global Chip Select.
TIO[10]/ MWEJ[1]	Y20	I/O	SRAM Tag[10] or another copy of MWEJ.
TIO[9]/ SRASJ[1]	Y19	I/O	SRAM Tag[9] or synchronous DRAM (SDRAM) RAS copy 1.
TIO[8]/ SCASJ[1]	W19	I/O	SRAM Tag[8] or synchronous DRAM (SDRAM) CAS copy 1.
TIO[7:0]	Y18, W18, V18, T14, V17, U17, U16, P16	I/O	SRAM Tag[7:0]. This pin contains the L2 tag address for 256 KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512 KB caches.
TWEJ	V16	O	Tag Write Enable. This signal, when asserted, writes into the external tag new state and tag addresses.
PCI Interface			
AD[31:28] AD[27:24] AD[23:20] AD[19:16] AD[15:12] AD[11:08] AD[07:04] AD[03:00]	A2, B2, A3, B3, A4, B4, C4, D6, B5, C5, A6, B6, C6, A7, B7, C7, C8, A9, B9, C9, A10, B10, C10, A11, C11, A12, B12, C12, A13, B13, A14, A15	I/O	PCI Address-and-Data Bus Lines. These lines connect to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	A5, A8, B8, B11	I/O	PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	E6	I/O	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access.
DEVSELJ	E9	I/O	Device Select. When the target device has decoded the address as its own cycle, it asserts DEVSELJ.
IRDYJ	E7	I/O	Initiator Ready. This indicates the initiator is ready to complete the current data phase of transaction.

Table 2-2 M1521 Signal Descriptions (continued)

Signal	Pin	Type	Description
TRDYJ	E8	I/O	Target Ready. This indicates the target is ready to complete the current data phase of transaction.
STOPJ	E11	I/O	Stop. This indicates the target is requesting the master to stop the current transaction.
LOCKJ	E5	I/O	Lock Resource Signal. This indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	D13, D11, D9, D7	I	Bus request signals of PCI Masters. When asserted, it means the PCI master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	D14, D12, D10, D8	O	Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the bus.
PHLDJ	D4	I	PCI bus hold request. This active low signal is a request from M1523 for the PCI bus.
PHLDAJ	D5	O	PCI bus hold acknowledge. This active low signal grants PCI to M1523.
PAR	E12	I/O	Parity bit of PCI buses. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ	E13	O	System Error. If the M1521 detects parity errors in DRAMs, it asserts SERRJ to notify the system.
Clock, Reset, and Suspend Interfaces			
RSTJ	T15	I	System Reset. This pin, when asserted, resets the M1521 and sets the register bits to their default values.
SUSPENDJ	P6	I	Suspend. When actively sampled, the M1521 enters the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
HCLKIN	K16	I	CPU Bus Clock Input. This signal is used by all of the M1521 logic that is in the host clock domain.
PCLKIN	E10	I	PCI Bus Clock Input. This signal is used by all of the M1521 logic that is in the PCI clock domain.
32K	W17	I	The refresh reference clock of frequency 32khz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.
UMA Interface			
MREQJ/ REQJ[4]	H6	I	Memory Request. This input signal is from the GUI device's MREQJ output. This pin can also be used as bus request signal of the fifth PCI master.

Table 2-2 M1521 Signal Descriptions (continued)

Signal	Pin	Type	Description
UMA Interface			
MGNTJ/ GNTJ[4]	F7	O	Memory Grant. This output connects to the MGNTJ of the GUI device. This pin can also be used as grant signal of the fifth PCI master.
PRIO	G15	I	Priority. The high priority request from the GUI device.
Power Pins			
VCC	F5, F6, G6, R6, R7, F14, F15, P15, R15, R16	P	Vcc 3.3V
VDD_5	E14	P	Vcc 5.0V
Vss or Gnd	E15, T16, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12	P	Ground

2.3 ALI M1523

The M1523 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1523 has Integrated System Peripherals (ISP) on-chip and provides advanced features in the DMA controller. This chip contains the keyboard controller, real-time clock and IDE master controller. This chip also supports the Advanced Programmable Interrupt controller (APIC) interface.

One eight-byte bidirectional line buffer is provided for ISA/DMA master memory read/writes. One 32-bit wide posted-write buffer is provided for PCI memory write cycles to the ISA bus. It also supports a PCI to ISA IRQ routing table and level-to-edge trigger transfer.

The chip has two extra IRQ lines and one programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD-ROMs. The ATA bus pins are dedicated to improve the performance of IDE master.

The M1523 supports the Super Green feature for Intel and Intel compatible CPUs. It implements programmable hardware events, software event and external switches (for suspend/turbo/ring-in). The M1523 provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control.

2.3.1 Features

- Technology
  - 0.6µm, triple-metal CMOS process
- Provides a bridge between the PCI bus and ISA bus
  - PCI interface
  - Supports PCI master and slave interface
  - Supports PCI master and slave initiated termination
  - PCI spec. 2.1 compliant (delay transaction support)
- Buffers
  - 8-byte bidirectional line buffers for DMA/ISA memory read/write cycles to PCI bus
  - 32-bit posted-write buffer for PCI memory write and I/O data write (for sound card) to ISA bus
- Provides steerable PCI interrupts for PnP PCI devices
  - Up to eight PCI interrupts routing
  - Level-to-edge trigger transfer
- Enhanced DMA controller
  - Provides seven programmable channels (four for 8-bit data size, three for 16-bit data size)

- 32-bit addressability
- Provides compatible DMA transfers
- Provides type F transfers

- Interrupt controller
  - Provides 14 interrupt channels
  - Independently programmable level/edge triggered channels
- Counter/Timers
  - Provides 8254 compatible timers for system timer, refresh request, speaker output use
- Keyboard controller
  - Built-in PS2/AT keyboard controller
  - The specific I/O is used to save the external TTL buffer
- Real time clock
  - Built-in real-time clock
  - 128-byte CMOS RAM with 2μA standby current maximum
- Plug-and-Play port support
  - programmable chip select
  - Steerable interrupt request lines
- PMU interface
  - Supports CPU SMM mode, SMI feature
  - Supports programmable stop clock throttle
  - Supports the APM control
  - Provides external suspend mode switch/turbo switch/ring-in switch
  - Provides four system states for power saving (on, doze, standby, suspend)
  - Provides three timers from 1 second to 300 minutes to individually monitor VGA, MODE, IN status
  - Supports RTC alarm wake up control
- IDE interface
  - Built-in PCI IDE master controller
  - Supports PIO modes up to mode 5 timings, and multiword DMA mode 0, 1, 2
  - 8 x 32-bit pre-read and posted-write buffers
  - Dedicated pins for ATA interface
- Supports up to 256 KB ROM size decode
- Reserved USB interface
- 208-pin PQFP package

2.3.2 Block Diagram

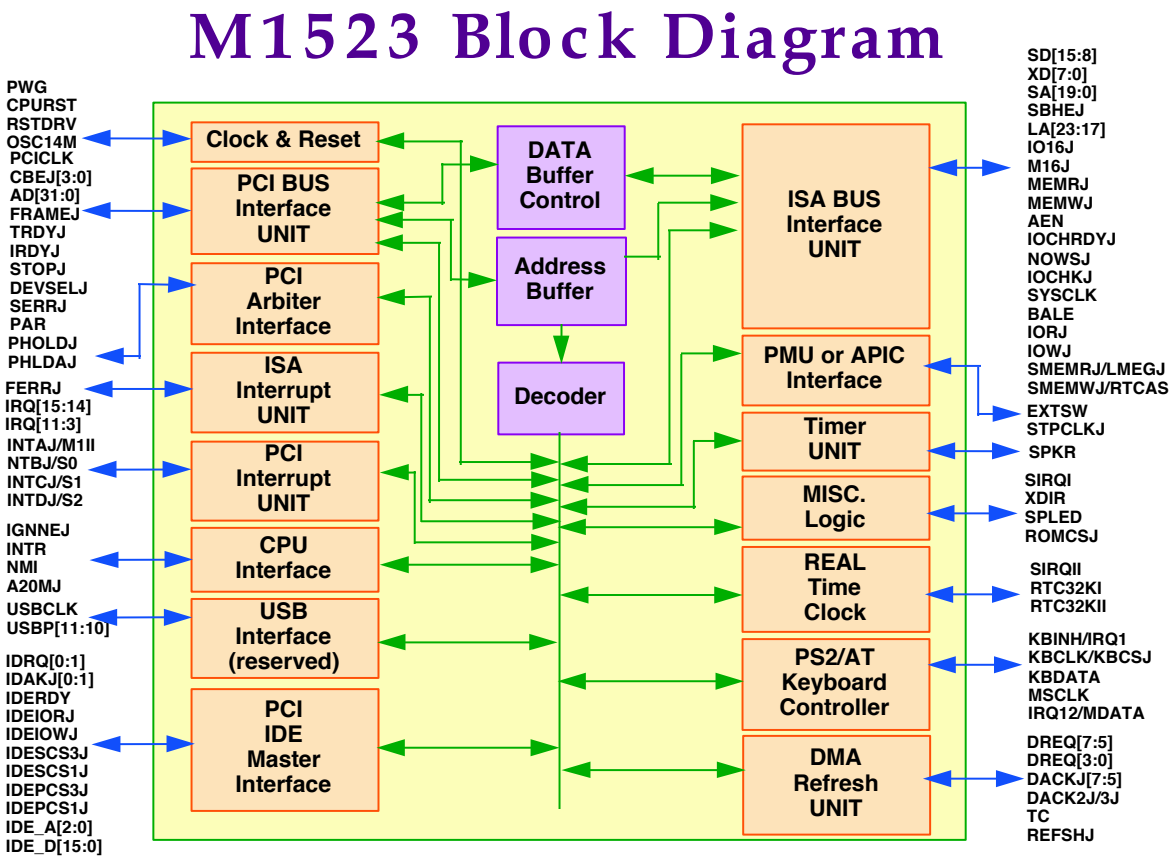


Figure 2-5 M1523 Block Diagram

2.3.3 Pin Diagram

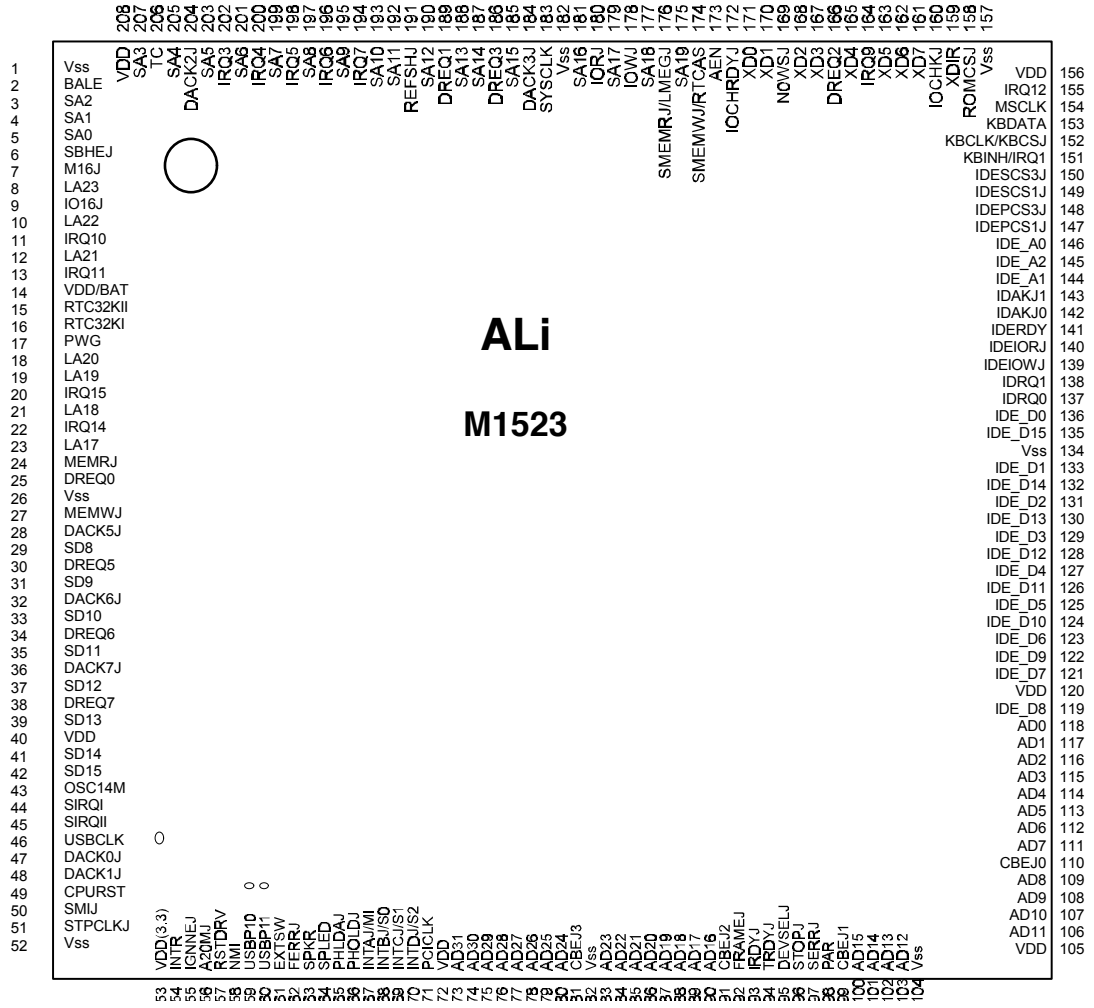


Figure 2-6 M1523 Pin Diagram

2.3.4 Signal Descriptions

Table 2-3 M1523 Signal Descriptions

Signal	Pin	Type	Description
Clock and Reset			
PWG	17	I	Power-Good Input. This signal comes from the power supply to indicate that power is available and stable.
CPURST	49	O	CPU Reset includes cold and warm reset 3.3V signal (connected to CPU INIT)
RSTDRV	57	O	CPU Cold Reset. 3.3V signal (connected to CPU RESET)
OSC14M	43	I	14.318Mhz Clock Input. This is used for 8254 timer clock.
PCI Interface			
PCICLK	71	I	PCI clock for internal PCI interface.
AD[31:0]	73-80, 83-90, 100-104, 106-109, 111-118	I/O	Address and Data are multiplexed on PCI bus. During the first clock of a PCI transaction, AD[31-0] contains a physical address. During subsequent clocks, AD[31-0] contains data.
C/BEJ[3:0]	81, 91, 99, 110	I/O	Bus Command and Byte Enable. During address phase, CBEJ[3:0] define the bus command. During data phase, CBEJ[3:0] define the byte enables.
FRAMEJ	92	I/O	Cycle Frame. is driven by current initiator to indicate the beginning and duration of an access.
DEVSELJ	95	I/O	Device Select. . This indicates that the target device has decoded the address as its own cycle. This pin is an output pin when the M1523 acts as a PCI slave that has decoded address as its own cycle including subtractive decoding.
IRDYJ	93	I/O	Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
TRDYJ	94	I/O	Target Ready indicates the target's ability to complete the current data phase of the transaction.
STOPJ	96	I/O	Stop indicates to the M1523 is requesting a master to stop the current transaction.
PAR	98	I/O	Parity Signal. PAR is even parity and is calculated on AD[31:0] and CBEJ[3:0]. When the M1523 acts as a PCI master, it drives PAR one PCI clock after address phase for a read/write transaction and one PCI clock after data phase for a write transaction. When the M1523 acts as target, it drives PAR one PCI clock after data phase for a PCI master read transaction.
SERRJ	97	I	System Error may be pulsed active by any agent that detects a system error condition. When SERRJ is sampled low, the M1523 asserts NMI to send an interrupt to the CPU.

Table 2-3 M1523 Signal Descriptions (continued)

Signal	Pin	Type	Description
PCI Interrupt Unit			
INTAJ_MI	67	I	PCI Interrupt Input A or PCI interrupt polling input.
INTBJ	68	I/O	PCI Interrupt Input B or polling select_0 output.
INTCJ	69	I/O	PCI Interrupt Input C or polling select_1 output.
INTDJ	70	I/O	PCI Interrupt Input D or polling select_2 output.
PCI Arbiter			
PHOLDJ	66	O	M1523 requests the ownership of the PCI bus. Hardware setting option Pull low : internal RTC is enabled Pull high : external RTC is used.
PHLDAJ	65	I	PCI Hold Acknowledge. When this pin is asserted, the M1523 owns the PCI bus.
CPU Interface (3.3V)			
IGNNEJ	55	O	Ignore Numeric Error. This pin is used as the ignore numeric coprocessor error.
INTR	54	O	Interrupt Request to CPU. This is the interrupt signal generated by the internal 8259.
NMI	58	O	Non-maskable Interrupt. This is non-maskable interrupt request to CPU.
A20MJ	56	O	CPU A20 Mask. This is the address line 20 mask signal.
ISA Interface			
FERRJ/IRQ13	62	I	Floating Point Error. FERRJ input to generate IRQ13. When the coprocessor interface is disabled in configuration port 43h bit 6, the function of this pin is IRQ13.
IRQ12 / MDATAO	155	I/O	Mouse Interrupt Request Input/Mouse Data Output. When internal PS/2 keyboard is disabled, this pin is mouse interrupt input. Otherwise, this pin is mouse data output.
IRQ[15:14], IRQ[11:9], IRQ[7:3]	20, 22, 13, 11, 164, 194, 196, 200, 202	I	Interrupt Request Signals.
SD[15:8]	42, 41, 39, 37, 35, 33, 31, 29	I/O	ISA High-byte Slot Data Bus. These lines are system data lines.
XD[7:0]	161-163, 165, 167, 168, 170-171	I/O	External Data Bus lines connect to SD[7:0] by an external TTL LS245, whose direction is controlled by the M1523 output signal XDIR.
SA19	175	O	ISA Slot Address Bus A19.
SA18	177	O	ISA Slot Address Bus A18.
SA17	179	O	ISA Slot Address Bus A17.

Table 2-3 M1523 Signal Descriptions (continued)

Signal	Pin	Type	Description
ISA Interface			
SA[16:0]	181, 185, 187, 188, 190, 192, 193, 195, 197, 199, 201, 203, 205, 207, 3, 4, 5	I/O	ISA Slot Address Bus. These lines are addresses connected to slot address.
SBHEJ	6	I/O	ISA Slot Byte-high Enable. In a CPU or PCI master cycle, this signal is generated by BE3J-BE0J and the chip's internal control circuit. In a DMA cycle, it is generated by internal 8237. In a refresh cycle, it is generated by the internal refresh circuits. It is an input signal for ISA master cycle.
LA[23:17]	8, 10, 12, 18, 19, 21, 23	I/O	ISA Latched Address Bus. They are input during ISA master cycle.
IO16J	9	I	ISA 16-bit I/O Device Indicator. This signal indicates the I/O device supports 16-bit transfers.
M16J	7	I/O	ISA 16-bit Memory Device Indicator. This signal indicates the memory device supports 16-bit transfers.
MEMRJ	24	I/O	ISA Memory Read. This signal is an input during ISA master cycle.
MEMWJ	27	I/O	ISA Memory Write. This signal is an input during ISA master cycle.
AEN	173	O	ISA I/O Address Enable. Active high signal during DMA cycle to prevent I/O device from misinterpreting the DMA cycle as valid I/O cycle.
IOCHRDY	172	I/O	ISA System Ready. This signal is an output during ISA/DMA master cycle.
NOWSJ	169	I	ISA Zero-wait State for Input. This signal terminates the CPU to ISA command instantly.
IOCHKJ	160	I	ISA Parity Error. M1523 generates NMI to CPU when this signal is asserted.
SYSCLK	183	O	ISA System Clock. This signal provides clocking function to ISA bus.
BALE	2	O	Bus Address Latch Enable. BALE is active throughout DMA and ISA master and refresh cycles.
IORJ	180	I/O	ISA I/O Read. This signal is an input during ISA master cycle.
IOWJ	178	I/O	ISA I/O Write. This signal is an input during ISA master cycle.

Table 2-3 M1523 Signal Descriptions (continued)

Signal	Pin	Type	Description
ISA Interface			
SMEMRJ / LMEGJ	176	O	ISA System Memory Read. When the internal RTC is enabled, this signal indicates that the memory read cycle is for an address below 1-MB address. Otherwise, this pin only indicates an address below 1M byte.
SMEMWJ / RTCAS	174	O	ISA System Memory Write. When the internal RTC is enabled, this signal indicates that the memory write cycle is for an address below 1-MB address. Otherwise, this pin is used as RTC address strobe.
DREQJ[7:5] DREQJ[3:0]	38, 34, 30, 186, 166, 189, 25	I	DMA Request Signals. These are DMA request input signals.
DACKJ[7:5] / DAK_SEL[2:0] DACKJ[3] / PCSJ, DACKJ[2] / DACKOJDACKJ[1], DACKJ[0]	36,32, 28, 184, 204, 48, 47	O I/O O	When DACKJ polling mode is disabled, these pins are DACKJ[7:5,3:0](O). Otherwise, these pins are DAK_SEL[2:0](O) connect to external MUX select inputs, PCSJ(O) programmable chip select, and DACKOJ(O) connected to external MUX chip enable.
TC	206	O	DMA End of Process. Hardware setting options: Pulled low: Support external I/O APIC mode Pulled high: Not support external I/O APIC
REFSHJ	191	I/O	ISA Refresh Cycle. This signal is input during ISA master cycles, but an output during other cycles.
Timer			
SPKR	43	O	Speaker Output. Hardware setting options: Pulled low: Enable Internal KBC Pulled high: Disable Internal KBC
Miscellaneous			
SPLED	44	O	Speed LED Output. Hardware setting options: Pulled low: Enable DMA DACKJ[7:5,3:0] polling mode Pulled high: Disable DMA DACKJ[7:5;3:0] polling mode
ROMCSJ	158	O	ROM and RTC Chip Select. This signal must be pulled high for normal operation.
XDIR	159	O	X-bus Direction Control. Hardware setting option: must be pulled high.
KBINH/ IRQ1	151	I	KB Inhibit Input when the internal KBC is enabled. IRQ1 Input when the internal KBC is disabled
KBCLK/ KBCSJ	152	I/O	KB interface CLK when the internal KBC is enabled. KB Chip Select when the internal KBC is disabled
KBDATA	153	O	KB interface Data when the internal KBC is enabled.

Table 2-3 M1523 Signal Descriptions (continued)

Signal	Pin	Type	Description
Miscellaneous			
MSCLK	154	O	Mouse Clock Output when the internal KBC is enabled.
RTC32KI	16	I	RTC 32.768K Osc1. This is crystal input and requires an external 32.768khz quartz crystal.
RTC32KII	15	I	RTC 32.768K Osc2. This is crystal input and requires an external 32.768khz quartz crystal.
SIRQI	44	I	Steerable IRQ Input 1
SIRQII/IRQ8J	45	I	Steerable IRQ Input 2 when the internal RTC is enabled. RTC interrupt input when the internal RTC is disabled.
USBCLK	46	I	Universal serial bus clock pin (reserved).
USBP1[1:0]	59, 60	I/O	Universal serial bus data pin (reserved).
Power Management			
EXTSW / APICREQJ	61	I	External SMI Switch or APIC Request Input. EXTSW is a falling edge triggered input to the M1523 showing that an external device is requesting the system to enter SMM mode. An external pull-up should be placed on this signal if it is not used or it is not guaranteed to be always driven. When external APIC mode is enabled, this pin is APICREQJ.
SMIJ / APICCSJ	50	O	SMM Interrupt or APIC Chip Select. A synchronous output asserted by the M1523 in response to one of many enabled hardware or software events. When external APIC mode is enabled, this pin is APICCSJ.
STPCLKJ / APICGNTJ	51	O	Stop CPU Clock Request or APIC Grant Output. STPCLKJ is connected directly to the CPU and is synchronous with PCI clock. When external APIC mode is enabled, this pin is APICGNTJ.
IDE Interface			
IDRQ[1:0]	138-137	I	IDE DRQ Request for IDE Master
IDAKJ[1:0]	143-142	O	IDE DACKJ for IDE Master
IDERDY	141	I	IDE Ready
IDEIORJ	140	O	IDE IORJ Command
IDEIOWJ	139	O	IDE IOWJ Command
IDESCS1J	149	O	IDE chip Select for Secondary Channel 0
IDESCS3J	150	O	IDE chip Select for Secondary Channel 1
IDEPCS1J	147	O	IDE chip Select for Primary Channel 0
IDEPCS3J	148	O	IDE chip Select for Primary Channel 1
IDE_A[2:0]	145, 144, 146	O	IDE ATA Address Bus

Table 2-3 M1523 Signal Descriptions (continued)

Signal	Pin	Type	Description
IDE Interface			
IDE_D[15:0]	135, 132, 130, 128, 126, 124, 122, 119, 121, 123, 125, 127, 129, 131, 133, 136	I/O	IDE ATA Data Bus
Vcc and Vss			
VCC3	53	P	Vcc 3.3V
VCC5/V_{BAT}	14	P	RTC Battery Input
VCC5	40, 72, 105, 120, 156, 208	P	VCC 5.0V(VDD)
Vss	1, 26, 52, 82, 104, 134, 157, 182	P	Vss or Ground.

2.4 ALI M7101 (Power Management Unit)

2.4.1 Features

- Four operating states - ON, DOZE, SLEEP, APM
- Programmable DOZE and SLEEP timer
- Programmable EL timer for backlight control
- Two Programmable APM timers
- Two output pins depending on operating state, each pin is programmable and power configurable
- Provides system activity and EL activity monitorings, includes
  - Video
  - Harddisk
  - Floppy
  - Serial port
  - Parallel port
  - Keyboard
  - Six programmable I/O address groups activity monitor
  - Two programmable memory address groups activity monitor
- Multiple external wake-up events from DOZE or SLEEP to ON states
  - External Push button
  - Cover open
  - Modem Ring
  - RTC alarm
  - DRQ
- Two level battery warning monitors
- 24 General Purpose I/O pins. Each pin can be programmed to become input or output
- 32 External expandable general purpose output signals
- 32 External expandable general purpose input signals
- LCD control
- Rundown monitor detect
- Suspend wake-up detect
- 100-pin PQFP package

2.4.2 Pin Diagram

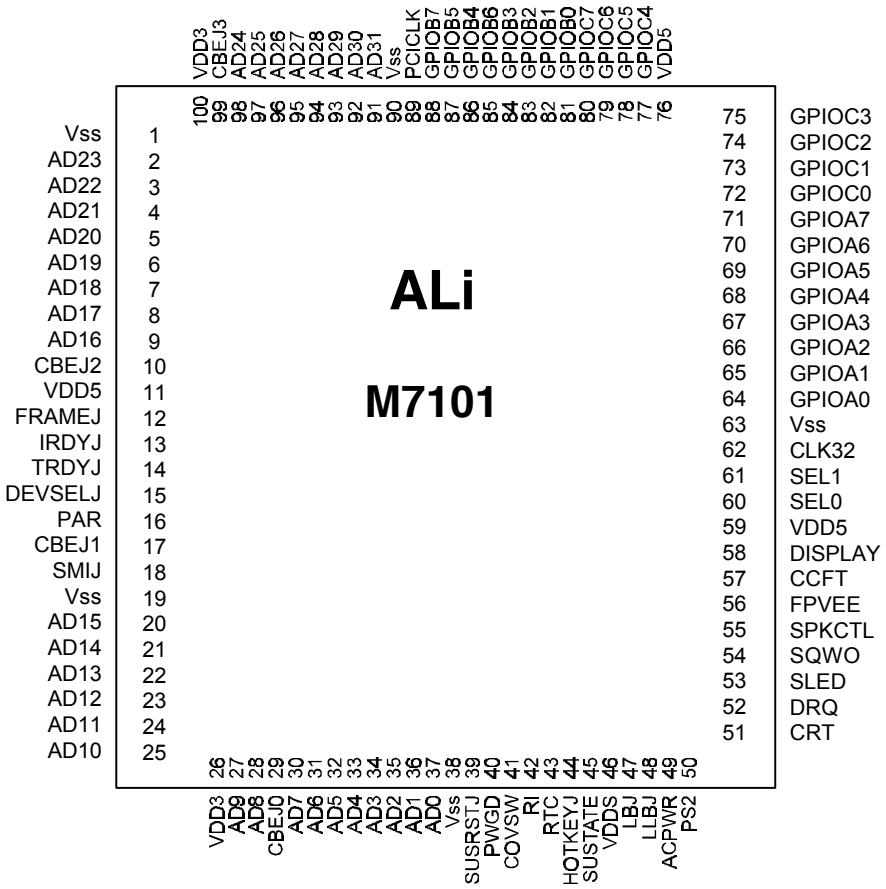


Figure 2-7 M7101 Pin Diagram

2.4.3 Pin Description

Table 2-4 M7101 Pin Descriptions

Name	No.	Type	Description
PCI interface : (42)			
PCICLK	89	I	PCI Clock. This is the PCI Bus interface CLK input signal. This clock frequency should not be more than 33 Mhz. It is used by internal PCI interface.
AD[31:0]	91-98,2-9, 20-25, 27, 28, 30-37	I/O	PCI Address and Data bus. These lines are connected to PCI Bus' AD[31:0]. These lines contain Address and Data bus information for PCI transaction.
CBEJ[3:0]	99,10, 17,29	I	PCI Bus Command and Byte enable. These are PCI bus commands at address phase and byte enable signals at data phase. Since M7101 is PCI slave only, it will not drive CBEJ[3:0]. They are inputs only.
FRAMEJ	12	I	Cycle FRAME for PCI bus. This signal indicates the beginning and duration of a PCI access.
DEVSELJ	15	O	Device select. When M7101 has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	13	I	Initiator Device Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	14	O	Target Device Ready. This signal indicates that M7101 is ready to complete the current data phase of transaction.
PAR	16	O	Parity bit of PCI bus. It is the even parity bit across AD[31:0] and CBEJ[3:0]
CLK & RESET interface : (3)			
CLK32	62	I	32KHz clock. This is 32KHz clock input, used by internal timers and relative PMU circuit.
PWGD	40	I	POWER GOOD. When PWGD low means the VDD5&VDD3 power supply is turned off. When high, it means the power is available and stable. This signal will be sent to suspend circuit to disable the suspend protected circuit when PWGD is high. It will also be sent to reset the circuit supplied by VDD5&VDD3 power.
SUSRSTJ	39	I	SUSPEND RESET. SUSPEND circuit RESET signal. When low, the suspend circuit will be reset. The suspend circuit is supplied by the VDDS power.
PMU Input event interface : (11)			
ACPWR	49	I	AC power. When plugged in or out, the AC adapter status will be reflected at this signal. Both low to high or high to low transition will generate SMIJ. An internal debounce is built-in to avoid the input bouncing problem. Both rising & falling will be detected. This is a smith-trigger input signal.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
PMU Input event interface : (11)			
LBJ	47	I	Low Battery. First stage battery low indication. If low is detected and Low Battery Timer is timeout, then battery low 1 SMIJ will be generated every programmed interval time until battery low 2 SMIJ is asserted or LB timer is reset. No debounce circuit is built in. Only low level is detected.
LLBJ	48	I	Low Low Battery. Second stage battery low indication. If low is detected and Low Low Battery Timer is timeout, then battery low 2 SMIJ will be generated every programmed interval time until both LB and LLB timer are reset. No debounce circuit is built in. Only low level is detected. LLBJ LBJ H H Normal condition H L Low Battery SMIJ will generate every interval. Low Low Battery SMIJ will not happen. L X Low Battery SMIJ will not happen. Low Low Battery SMIJ will generate every interval.
COVSW /SUSTAT2	41	I/O	Cover switch (when 0F8h, D7=1). Cover switch status input. When COVER is closed, the cover switch is also pressed and a COVSW SMIJ will be generated. When COVER is opened, the cover switch will be released, a COVSW SMIJ will be generated, too. Moreover, both close and open will generate a doze-to-on or sleep-to-on SMIJ to wake the system up if the system is in Doze or Sleep state, respectively. Debounce circuit is built in. It detects both rising and falling edge. Suspend status 2 (when 0F8h, D7=0, it is default value). It is suspend status 2 signal during 0/5V suspend system. It will be low in normal. When writing to port 0FAh, it will go high to close the charger. Any event of RI, RTC or HOTKEYJ will wake it up, and let this pin go low again.
RI	42	I	Modem Ring. Modem ring input. A programmable ring counter will count the ring pulse. If the ring pulse reaches the counter‘s setting value, a doze-to-on SMIJ or sleep-to-on SMIJ will be generated to wakeup the system. If the system is already at on state, there will be no new event or action. No debounce circuit is built in. It only detects rising edge.
RTC	43	I	RTC Alarm wakeup. A low to high transition of this signal will generate a doze-to-on or sleep-to-on SMIJ to wakeup the system. If the system is already at on state, there will be no new event or action. No debounce circuit is built in. It only detects rising edge.
DRQ	52	I	Floppy DMA Request. A low to high transition of this signal will generate a doze-to-on or sleep-to-on SMIJ to wakeup the system. If the system is at on state already, there will be no new event or action. No debounce circuit is built in. It only detects rising edge.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
PMU Input event interface : (11)			
PS2	50	I	External PS2 MOUSE. This signal represents whether the PS2 MOUSE is plugged in or not. When a PS2 MOUSE is plugged in, a high to low transition will generate a SMIJ. When a PS2 MOUSE is pulled out, a low to high transition will generate a SMIJ as well. In addition, the signal status can be read from BEEPER offset 0CBh D1 register. Debounce circuit is built in. It detects both rising and falling edges. This is a Smith-trigger input signal.
CRT	51	I	External CRT connector. This signal represents whether the External CRT connector is plugged in or not. When an external CRT connector is plugged in, a high to low transition will generate an SMIJ. When an external CRT connector is pulled out, a low to high transition will generate an SMIJ, too. Moreover, the signal status can be read from BEEPER offset 0CBh D0 register. Debounce circuit is built in. It detects both rising and falling edges. Smith-trigger input.
HOTKEYJ	44	I	HotKey press. When HotKey is pressed, a high to low transition will generate an SMIJ. Debounce circuit is built in. It detects only falling edge. This is a Smith-trigger input signal.
FPVEE	56	I	LCD backlight VEE. LCD backlight VEE on/off control signal. Internal circuit uses this signal to generate DISPLAY and CCFT signals. On one hand, if FPVEE goes from low to high, DISPLAY will go high after 62.5ms to 125ms. If FPVEE goes low, DISPLAY will go low immediately. On the other hand, FPVEE will AND with offset 0D2h D0 to generate CCFT. That is, if both FPVEE and offset 0D2h D0 are high then CCFT will be high or 1Khz clock with programmable duty cycle. Otherwise CCFT will be low.
PMU output interface (9)			
SLED	53	O	Square LED display. 1Hz/2Hz square wave output. It can drive the LED to Flash. When disabled, this signal will be kept at high/low level as programmed.
SPKCTL	55	O	Speaker output. This signal is connected to speaker circuit to generate sound directly.
SQWO	54	O	Square wave output. Square wave output with 1Hz or 2Hz. When disabled, this signal will keep at high/low level as programmed.
SEL[1:0]	61-60	I/O	Programmable output control. These two pins are programmable output control pins at different state. When Power on, these two pins will be inputs and the Pull high(internal chip default is pull high 50K) or pull low (The pull low should use 4.7K resistor), will latch to ON state register. The values of ON, DOZE and SLEEP registers corresponding to four operation status can be programmed. That is, when system is at different states, the corresponding register value will be sent to SEL[1:0].

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
PMU output interface (9)			
CCFT	57	O	Backlight control. This signal is used to turn on/off LCD backlight. FPVEE will AND with offset 0D2h D0 to generate CCFT. That is, if both FPVEE and offset 0D2h D0 are high then CCFT will be high or 1Khz signal with programmed duty cycle by offset 0Fbh D[4:0]. Otherwise CCFT will be low.
DISPLAY	58	O	LCD Display On/Off control. This signal is used to control the LCD display ON/OFF. If FPVEE goes from low to high, DISPLAY will also go high after a period of about 62.5ms to 125ms. If not active, it will go low immediately.
SMIJ	18	O	System Management Interrupt. System Management interrupt output. It is the SMIJ output when internal SMIJ is generated or the IN_SMIJ input of the APM function is asserted. The high/low active level can be selected. There are three types of active method : 1. If offset 0D2h D7=1,D3=0, this signal will be asserted until reading/writing all of SMIJ status register‘s bits. This can be treated as a level SMIJ. 2. If offset 0D2h D7=0, D3=1, this signal will be asserted until reading/writing all of SMIJ status register‘s bits or a programmed interval time out. 3. If offset 0D2h D7=0, D3=0, this signal will be asserted for an interval time. This can be treated as a pulse SMIJ.
SUSTATE	45	O	SUSPEND STATE. When writing to port 0FAh or POSSTA goes high, the SUSTATE will go high. The system will enter SUSPEND mode. Only VDDS will supply the power, other VDD5 or VDD3 will have no power. Only RI, RTC, HOTKEYJ or COVSW can wake up the system and let the SUSTATE be low again. The VDD5 and VDD3 will supply power.
General purpose I/O interface(24)			
General purpose I/O group A			
GPIOA[7:0]	71-64	I/O	General Purpose I/O group A. These signals can be programmed to be inputs or outputs. Offset 0D9h D[7:0] control the I/O attributes. When programmed to be outputs, offset 0D8h D[7:0] will be set to corresponding signal. When programmed to be inputs, the signal can be read from the Offset 0D8h D[7:0] corresponding bits. Offset 0D9h D[n] = 0 GPIOA[n]= Input GPIOA[n] value can be read from Offset 0D8h D[n] 1 GPIOA[n]= Output Offset 0D8h D[n] value will be sent to GPIOA[n] where "n" is from 7 to 0
GPIOA7 /POSSTA	(71)	I	Positive input. When offset 0F6h D13=‘1’, this pin will sense a high level to active SUSTATE pin and force M7101 input suspend mode.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
General purpose I/O interface(24)			
General purpose I/O group A			
GPIOA6 /SPEKIN	(70)	I	Speak input. When offset 0F6h D6='1', this pin will be speaker input. The input signal will xor with SPKCTL internally.
GPIOA5 /GPIOWB	(69)	O	External General Purpose I/O B write. When SQWO is pull low 4.7K, the GPIOA5 will become GPIOWA. External General purpose A R/W control pulse, When write index 0F0h with a byte or a word. A 74373 latch pulse will be generated at this pin. The 74373 input should be connected to PCI AD[23:16] if a byte command. If a word command, two 74373s will be used and inputs are connected to PCI AD[31:16]. The write action also will write into the internal register. So when reading the offset, the value will be sent by M7101 to host.
GPIOA4 /GPIORBJ	(68)	O	External General Purpose I/O B read. When SQWO is pull low 4.7K, the GPIOA0 will become GPIORAJ. External General purpose A Read control pulse. When Read index 0F1h with a byte or a word, a 74245 OEJ pulse will be generated at this pin. The 74245 output should be connected to PCI AD[23:16] if a byte command. If a word command, two 74245 will be used and4 outputs are connected to PCI AD[31:16]. When read index 0E1h, M7101 will send DEVSELJ, TRDYJ but float the AD[31:0] because the data will be sent by 74245. The write action has no meaning and nothing will be done.
GPIOA3 /CONTRAST2 /SLOWDOWN	(67)	O /O	Contrast2. When offset 0F6h D14='0' and D9='1', this pin will be the LCD contrast output 2. It is a 1Khz signal with programmable duty cycle controlled by offset 0FBh D[15:13]. SLOWDOWN (default). When offset 0F6h D14='1', this pin will be the slow down clock control output pin.
GPIOA2 /CONTRAST1	(66)	O	Contrast1. When offset 0F6h D14='0' and D8='1', this pin will be the LCD contrast output1. It is a 1 KHz signal with programmable duty cycle controlled by offset 0FBh D[12:8].
GPIOA1 /GPIOWA	(65)	O	External General Purpose I/O A write. When SPKCTL is pull low 4.7K, the GPIOA1 will become GPIOWA. External General purpose A R/W control pulse, When write index 0E0h with a byte or a word. A 74373 latch pulse will be generated at this pin, The 74373 input should be connected to PCI AD[23:16] if a byte command. If a word command , two 74373s will be used and inputs are connected to PCI AD[31:16]. The write action also will write into the internal register. So when reading the offset, the value will be sent by M7101 to host.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
General purpose I/O interface(24)			
General purpose I/O group A			
GPIOA0 /GPIORAJ	(64)	O	External General Purpose I/O A read. When SPKCTL is pull low 4.7K, the GPIOA0 will become GPIORAJ. External General purpose A Read control pulse, When Read index 0E1h with a byte or a word. A 74245 OEJ pulse will be generated at this pin. The 74245 output should be connected to PCI AD[23:16] if a byte command. If a word command, two 74245s will be used and outputs are connected to PCI AD[31:16]. When read index 0E1h, M7101 will send DEVSELJ, TRDYJ but float the AD[31:0] because the data will be sent by 74245. The write action has no meaning and nothing will be done.
General purpose I/O interface(24)			
General purpose I/O group B			
GPIOB[7 :0]	88,85, 87,86, 84-81	I/O	General Purpose I/O group B. These signals can be programmed to be input or output. Offset 0DBh D[7:0] control the I/O attribute. When programmed to be output, Offset 0DAh D[7:0] will set to corresponding signal. When programmed to be input, the signal can be read from the Offset 0DAh D[7:0] corresponding bits. Offset 0DBh D[n] = 0 : GPIOB[n]=input GPIOB[n] value can be read from Offset 0DAh D[n] 1 : GPIOB[n]=Output Offset 0DAh D[n] value will send to GPIOB[n] "n" value is from 7 to 0
GPIOB7 /STPCLKJ	(88)	O	Stop clock signal. When DISPLAY is pulled low or offset 0F6h D14='1', this pin will become stop clock signal output. It may be connected to CPU to force it into STPGNT or STPCLK mode. Write port 0EFh will assert this function.
GPIOB6 /AMSTATJ	(85)	O	APM State. When DISPLAY is pulled low, this pin will be APM state. It may be connected to clock generator to slow down clock. It is asserted when HALT or STPGNT cycle is detected and recovers when IN_SMIJ, IN_INTR or IN_INIT is asserted. System can use this signal to know the APM status, and slow down the speed or turn off some peripheral power to decrease the power consumption. This signal will be synchronized with PCICLK's rising or falling edge.
GPIOB5 /OUT_INIT	(87)	O	INIT Output. When DISPLAY is pulled low, this pin will be INIT output. It will be disabled when IN_INIT is detected and AMSTATJ is asserted. Then, it will be sent as a 16 PCICLK wide pulse after AMSTATJ is deasserted. Otherwise, it will be the same with IN_INIT. It may be connected to CPU.
GPIOB4 /OUT_INTR	(86)	O	INTR Output. When DISPLAY is pulled low, this pin will become INTR output. It may be connected to CPU. When AMSTATJ is asserted, IN_INTR will be masked until AMSTATJ is de-asserted.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
General purpose I/O interface(24)			
General purpose I/O group B			
GPIOB3 /IN_BRDYJ	(84)	I	BRDYJ Input. When DISPLAY is pulled low, this pin will be BRDYJ input. It must be connected to CPU.
GPIOB2 /IN_INIT	(83)	I	INIT Input. When DISPLAY is pulled low, this pin will be INIT input.
GPIOB1 /IN_SMIJ	(82)	I	SMIJ Input. When DISPLAY is pulled low, this pin will be SMIJ input.
GPIOB0 /IN_INTR	(81)	I	SMIJ Input. When DISPLAY is pulled low, this pin will be INTR input.
General purpose I/O interface(24)			
General purpose I/O group C			
GPIOC[7:0]	80-77, 75-72	I/O	General Purpose I/O group C. When these signals are set to GPIOC[7:0], these signals can be programmed to be input or output. Offset 0DDh D[7:0] control the I/O attribute. When programmed to be output, offset 0DCh D[7:0] will set to corresponding signal. When programmed to be input, the signal can be read from the Offset 0DCh D[7:0] corresponding bits. Offset 0DDh D[n] = 0 : GPIOC[n]=input GPIOC[n] value can be read from Offset 0DCh D[n] 1 : GPIOC[n]=Output Offset 0DAh D[n] value will send to GPIOC[n] "n" value is from 7 to 0
GPIOC7 /VCSJ	(80)	I	VGA Chip select. When offset 0F6h D12=0, this signal is GPIOC7. When D12=1, this signal will become VCSJ. When access to VGA memory range, VGA chip will set this signal to active low. The internal circuit use this signal to monitor the VGA active to restart the timer or generate SMIJ. No debounce is built in. Low level detect.
GPIOC6 /SETUPJ	(79)	I	Setup switch. When offset 0F6h D11=0, this signal is GPIOC6. When D11=1, this signal will become SETUPJ. Setup switch input. A transition will generate setup switch SMIJ. Debounce circuit is built in. Both rising and falling edges are detected. Smith-trigger input.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
General purpose I/O interface(24)			
General purpose I/O group C			
GPIOC5 /EXTSW	(78)		External suspend/resume switch. When offset 0F6h D10=0, this signal is GPIOC5. When D10=1, this signal will become EXTSW. External Suspend/Resume switch input. Pressing this switch will generate SMIJ to suspend or resume the system. When the system is at resume status(On, Doze), pressing this switch will enter Suspend status(Sleep). When the system is at Suspend status(Sleep), pressing the switch will enter ON status. Debounce circuit is built in. Both rising and falling edge are detected. Smith-trigger input.
GPIOC[4] /EJECT	(77)		External Eject SMIJ trigger. 1. When index 0F6h D7=0, this signal is GPIOC(4). When it is 1, this signal will become EJECT When a rising/falling edge happens at this input, an SMIJ will be generated. Built in debounce circuit.
GPIOC[3] /DOCKJ	(75)		Docking insert detected. When index 0F6h D7=0, this signal is GPIOC[3]. When it is 1, this signal will become DOCKJ When a rising/falling edge happens at this input, an SMIJ will be generated. Built in debounce circuit.
GPIOC[2] /BIOSA17	(74)		BIOS address ROM A17 When CCFT is low, this signal will become BIOSA17.
GPIOC[1] /BIOSA16	(73)		BIOS address ROM A16 When CCFT is low, this signal will become BIOSA16.
GPIOC[0] /ISA16	(72)		ISA SLOT address A16 When CCFT is pulled low, this signal will become ISA16. These two signals connect BIOS ROM A17 & A16 to distinguish the four parts of BIOS ROM and decided by offset 0D2h D[2:1]. D2 D1 ISA16 BIOSA17 BIOSA16 ROM region X X 1 0 1 1 X 0 0 0 0 0 0 1 0 1 0 2 1 1 0 1 1 3 We divided the 256K byte ROM into four parts. E region will occupy three parts--0,2,3, F region will occupy one part--1. So, when CPU accesses to F region, that is, ISA16=1, then system will access ROM region 1, F segment. The E region has three parts overlaying the same address, software can use offset 0D2h D[2:1] to choose which ROM region to be accessed.

Table 2-4 M7101 Pin Descriptions (Continued)

Name	No.	Type	Description
Power Pins			
VDD5 x 3	11,59,76	P	5V VDD input
VDD3 x 2	26,100	P	3.3V VDD input
VDDS x 1	46	P	5V Suspend VDD input. This pin supplies to RI, RTC, HOTKEYJ, COVSW, SUSTATE, PWGD, SUSRSTJ pad.
VSS x 5	1,19,38, 63,90	P	VSS Ground.

2.4.4 Different Pin definition setting

- SLED, CCFT, DISPLAY, SPKCTL, SQWO and GPIOC2 pins are all internal pull high 50K ohms. The blank part of following table means keeping the original pin definition.
- When SLED default is pulled high, the chip will be in normal mode.
- When SLED is pulled low by 4.7K resistor, the chip will be in test mode.
- When GPIOC2 pull low, the PCI ports are 0078/007A and offset 0F6h D15 will be set, otherwise, 0178/017A.

Table 2-5 M7101 Different Pin Definition Setting

Original pin definition	CCFT pull low 4.7K	DISPLAY pull low 4.7K	SPKCTL pull low 4.7K	SQWO pull low 4.7K
	offset 0F6h D1=1	offset 0F6h D2=1	offset 0F6h D3=1	offset 0F6h D4=1
GPIOA5				GPIOWB
GPIOA4				GPIORBJ
GPIOA1			GPIOWA	
GPIOA0			GPIORAJ	
GPIOB7		STPCLKJ		
GPIOB6		AMSTATJ		
GPIOB5		OUT_INIT		
GPIOB4		OUT_INTR		
GPIOB3		IN_BRDYJ		
GPIOB2		IN_INIT		
GPIOB1		IN_SMIJ		
GPIOB0		IN_INTR		
GPIOC2	BIOSA17			
GPIOC1	BIOSA16			
GPIOC0	ISA16			

When offset 0F6h, D5=1 and offset 0FBh, D7=1; GPIOB[7:0] and GPIOA[7:0] output some clocks for testing. The clocks are OTCOUNT, O16K, TCLK2, TCLK3, O128HZ, O16HZ, O8HZ, O4HZ, O2HZ, O1Hz, ELCOUNT, DZCOUNT, SLCOUNT, RICOUNT, LBCOUNT[1:0].

Table 2-6 M7101 Original Pin Definition Setting

Original pin definition	D6=1	D7=1	D8=1	D9=1	D10=1	D11=1	D12=1	D13=1	D14=1
GPIOA7								POSSTA	
GPIOA6	SPEKIN								
GPIOA3				CONTRAST2					SLOWDN
GPIOA2			CONTRAST1						
GPIOB7									STPCLKJ
GPIOB3									BRDYJ
GPIOC7							VCSJ		
GPIOC6						SETUP			
GPIOC5					EXTSW				
GPIOC4		EJECYJ							
GPIOC3		DOCKJ							

Following is the default pulled values of GPIOA, GPIOB and GPIOC :

- Pull high : GPIOA0, GPIOA4, GPIOB1, GPIOB3, GPIOB6, GPIOB7, GPIOC1, GPIOC2, GPIOC5, GPIOC6, GPIOC7.
- Pull low : Other GPIO pins.

2.4.5 Numerical Pin List

Table 2-7 M7101 Numerical Pin List

No.	Pin Name	Type
1	VSS	P
2	AD23	I/O
3	AD22	I/O
4	AD21	I/O
5	AD20	I/O
6	AD19	I/O
7	AD18	I/O
8	AD17	I/O
9	AD16	I/O
10	CBEJ2	I
11	VDD5	P
12	FRAMEJ	I
13	IRDYJ	I
14	TRDYJ	O
15	DEVSELJ	O
16	PAR	O
17	CBEJ1	I
18	SMIJ	O
19	VSS	P
20	AD15	I/O
21	AD14	I/O
22	AD13	I/O
23	AD12	I/O
24	AD11	I/O
25	AD10	I/O
26	VDD3	P
27	AD9	I/O
28	AD8	I/O
29	CBEJ0	I
30	AD7	I/O
31	AD6	I/O
32	AD5	I/O
33	AD4	I/O
34	AD3	I/O
35	AD2	I/O
36	AD1	I/O
37	AD0	I/O
38	VSS	P
39	SUSRSTJ	I
40	PWGD	I
41	COVSW	I/O
42	RI	I
43	RTC	I
44	HOTKEYJ	I
45	SUSTATE	O
46	VDDS	P
47	LBJ	I
48	LLBJ	I
49	ACPWR	I
50	PS2	I

No.	Pin Name	Type
51	CRT	I
52	DRQ	I
53	SLED	O
54	SQWO	O
55	SPKCTL	O
56	FPVEE	I
57	CCFT	O
58	DISPLAY	O
59	VDD5	P
60	SEL0	I/O
61	SEL1	I/O
62	CLK32	I
63	VSS	P
64	GPIOA0	I/O
65	GPIOA1	I/O
66	GPIOA2	I/O
67	GPIOA3	I/O
68	GPIOA4	I/O
69	GPIOA5	I/O
70	GPIOA6	I/O
71	GPIOA7	I/O
72	GPIOC0	I/O
73	GPIOC1	I/O
74	GPIOC2	I/O
75	GPIOC3	I/O
76	VDD5	P
77	GPIOC4	I/O
78	GPIOC5	I/O
79	GPIOC6	I/O
80	GPIOC7	I/O
81	GPIOB0	I/O
82	GPIOB1	I/O
83	GPIOB2	I/O
84	GPIOB3	I/O
85	GPIOB6	I/O
86	GPIOB4	I/O
87	GPIOB5	I/O
88	GPIOB7	I/O
89	PCICLK	I
90	VSS	P
91	AD31	I/O
92	AD30	I/O
93	AD29	I/O
94	AD28	I/O
95	AD27	I/O
96	AD26	I/O
97	AD25	I/O
98	AD24	I/O
99	CBEJ3	I
100	VDD3	P

2.4.6 Alphabetical Pin List

Table 2-8 M7101 Alphabetical Pin List

No.	Pin Name	Type
49	ACPWR	I
37	AD0	I/O
36	AD1	I/O
35	AD2	I/O
34	AD3	I/O
33	AD4	I/O
32	AD5	I/O
31	AD6	I/O
30	AD7	I/O
28	AD8	I/O
27	AD9	I/O
25	AD10	I/O
24	AD11	I/O
23	AD12	I/O
22	AD13	I/O
21	AD14	I/O
20	AD15	I/O
9	AD16	I/O
8	AD17	I/O
7	AD18	I/O
6	AD19	I/O
5	AD20	I/O
4	AD21	I/O
3	AD22	I/O
2	AD23	I/O
98	AD24	I/O
97	AD25	I/O
96	AD26	I/O
95	AD27	I/O
94	AD28	I/O
93	AD29	I/O
92	AD30	I/O
91	AD31	I/O
29	CBEJ0	I
17	CBEJ1	I
10	CBEJ2	I
99	CBEJ3	I
57	CCFT	O
62	CLK32	I
41	COVSW	I/O
51	CRT	I
15	DEVSELJ	O
58	DISPLAY	O
52	DRQ	I
56	FPVEE	I
12	FRAMEJ	I
64	GPIOA0	I/O
65	GPIOA1	I/O
66	GPIOA2	I/O
67	GPIOA3	I/O

No.	Pin Name	Type
68	GPIOA4	I/O
69	GPIOA5	I/O
70	GPIOA6	I/O
71	GPIOA7	I/O
81	GPIOB0	I/O
82	GPIOB1	I/O
83	GPIOB2	I/O
84	GPIOB3	I/O
85	GPIOB6	I/O
86	GPIOB4	I/O
87	GPIOB5	I/O
88	GPIOB7	I/O
72	GPIOC0	I/O
73	GPIOC1	I/O
74	GPIOC2	I/O
75	GPIOC3	I/O
77	GPIOC4	I/O
78	GPIOC5	I/O
79	GPIOC6	I/O
80	GPIOC7	I/O
44	HOTKEYJ	I
13	IRDYJ	I
47	LBJ	I
48	LLBJ	I
16	PAR	O
89	PCICLK	I
50	PS2	I
40	PWGD	I
42	RI	I
43	RTC	I
60	SEL0	I/O
61	SEL1	I/O
53	SLED	O
18	SMIJ	O
54	SQWO	O
55	SPKCTL	O
39	SUSRSTJ	I
45	SUSTATE	O
14	TRDYJ	O
26	VDD3	P
100	VDD3	P
59	VDD5	P
11	VDD5	P
76	VDD5	P
46	VDDS	P
1	VSS	P
19	VSS	P
38	VSS	P
63	VSS	P
90	VSS	P

2.4.7 Function Description

The function blocks of M7101 are as follows :

1. PCI Interface
2. State Controller
3. Timer
4. Wake up event handler
5. Activity monitor
6. Battery monitor
7. General Purpose Input/Output (GPIO)
8. SMIJ Generator
9. SUSPEND monitor
10. APM monitor
11. Rundown Emulation
12. LCD control
13. SLOWDOWN control

PCI interface

The PCI interface is running at PCICLK frequency. From the point of PCI bus, M7101 is a hidden component. There are no PCI configuration spaces built in. So using PCI configuration read/write method cannot detect the existence of M7101.

M7101 just decodes the I/O 0178h/017Ah or 0078h/007Ah address. When it detects the address, it will assert the DEVSELJ signal and TRDYJ when data is ready. M7101 is only a PCI slave device, no REQJ and GNTJ signal required. All the PCI interface timing can meet the requirements of PCI spec. V2.1.

M7101 will monitor the PCI bus behavior to detect the Device access like HDD, SIO, PIO, VGA memory range, Floppy, KBC and IO&MEM group. It will decode these addresses but not assert DEVSELJ. The interface is static design. So the input PCICLK can be changed from 33 MHz to 0 Hz without glitch.

There is a Lock register at offset 0D1h. When set D5 to 1 will unlock I/O port 017Ah/007Ah. Host can read or write I/O port 017Ah/007Ah. When set D5 to 0, then Host cannot I/O read/write I/O port 017Ah/007Ah except the offset 0D1h. No matter lock or unlock, when access to I/O port 017Ah, DEVSELJ will always be active.

Table 2-9 M7101 PCI Interface Lock Register

Action	I/O Port 0178h/0078h	I/O Port 017Ah/007Ah
Lock Read	not available except offset 0D1h	not available except offset 0D1h
Lock Write	not available except offset 0D1h	not available except offset 0D1h
Unlock Read	available	available
Unlock Write	available	available

State Machine for PCI Interface.

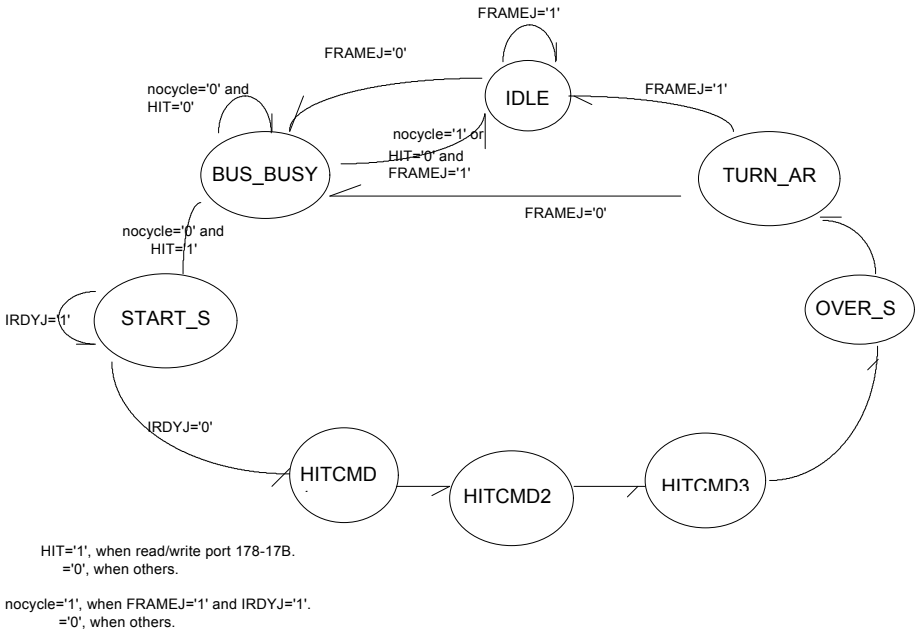


Figure 2-8 State Machine for PCI Interface

2.5 C&T 65550 High Performance Flat Panel/CRT VGA Controller

The C&T65550 of high performance multimedia flat panel / CRT GUI accelerators extend CHIPS' offering of high performance flat panel controllers for full-featured note books and sub-notebooks. The C&T65550 offers 64-bit high performance and new hardware multimedia support features.

2.5.1 Features

HIGH PERFORMANCE

Based on a totally new internal architecture, the C&T65550, integrates a powerful 64-bit graphics accelerator engine for Bit Block Transfer (BitBLT), hardware cursor, and other functions intensively used in graphical User Interfaces (GUIs) such as Microsoft Windows™. Superior performance is also achieved through a direct 32-bit interface to the PCI Local Bus. The C&T65550 offers exceptional performance when combined with CHIPS advanced linear acceleration driver technology .

HARDWARE MULTIMEDIA SUPPORT

The C&T65550 implements independent multimedia capture (and display systems on-chip. The capture system places data in display memory (usually off screen) and the display system places it in a window on the screen.

The capture system can receive data from either the system bus or from the ZV enabled video port in either RGB or YUV format. The input data can also scaled down before storage in display memory (c.g., from any size larger than 320x240 down to 352x248). Capture of input data may also be double buffered for smoothing and to prevent image tearing.

The display system can independently place either RGB or YUV data from any where in display memory into an on-screen window which can be any size and located at any pixel boundary (YUV data is converted to RGB "on-the-fly" on out put). Non-rectangular windows .are supported via color keying. The data can be functionally zoomed on output up to 8x to fit the onscreen window and can be horizontally and vertically inter polated to scale or zoom artifacts. Interlaced and non-interlaced data are supported in both capture and display systems.

VERSATILE PANEL SUPPORT

The C&T65550 supports a wide variety of monochrome and color Single-Panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD) standard and high-resolution passive STN and active matrix TFT/MIM LCD, and EL panels. For monochrome panels, up to 64 gray scales are supported. Up to 4096 different colors can be displayed on passive STN LCDs and up to 16M colors on 24-bit active matrix LCDs.

The C&T65550 offers a variety of programmable features to optimize display quality. Vertical centering and stretching are provided for handling modes with less than 480 lines on 480-line panels. Horizontal and vertical stretching capabilities are also available for both text and graphics modes for optimal display of VGA text and graphics modes on 800x600 and 1024x768 panels. Three selectable color-to-gray scale reduction techniques and SMARTMAP™ are available for improving the ability to view color applications on monochrome panels. CHIPS' polynomial FRC algorithm reduces panel flicker on a wider range of panel types with a single setting for a particular panel type.

LOW POWER CONSUMPTION

The C&T65550 employs a variety of advanced power management features to reduce power consumption of the display sub-system and extend battery life. Although optimized for 3.3V operation, The C&T65550 controller's internal logic. memory interface, bus interface, and panel interfaces can he independently configured to operate at either 3.3V or 5V.

SOFTWARE COMPATIBILITY/FLEXIBILITY

The C&T65550 are fully compatible with VGA at the register, and BIOS levels. CHIPS and third-party vendors supply fully VGA-compatible BIOS, end-user utilities and drivers for common application programs

Pin names in parentheses (...) indicate alternate functions.

2.5.2 Block Diagram

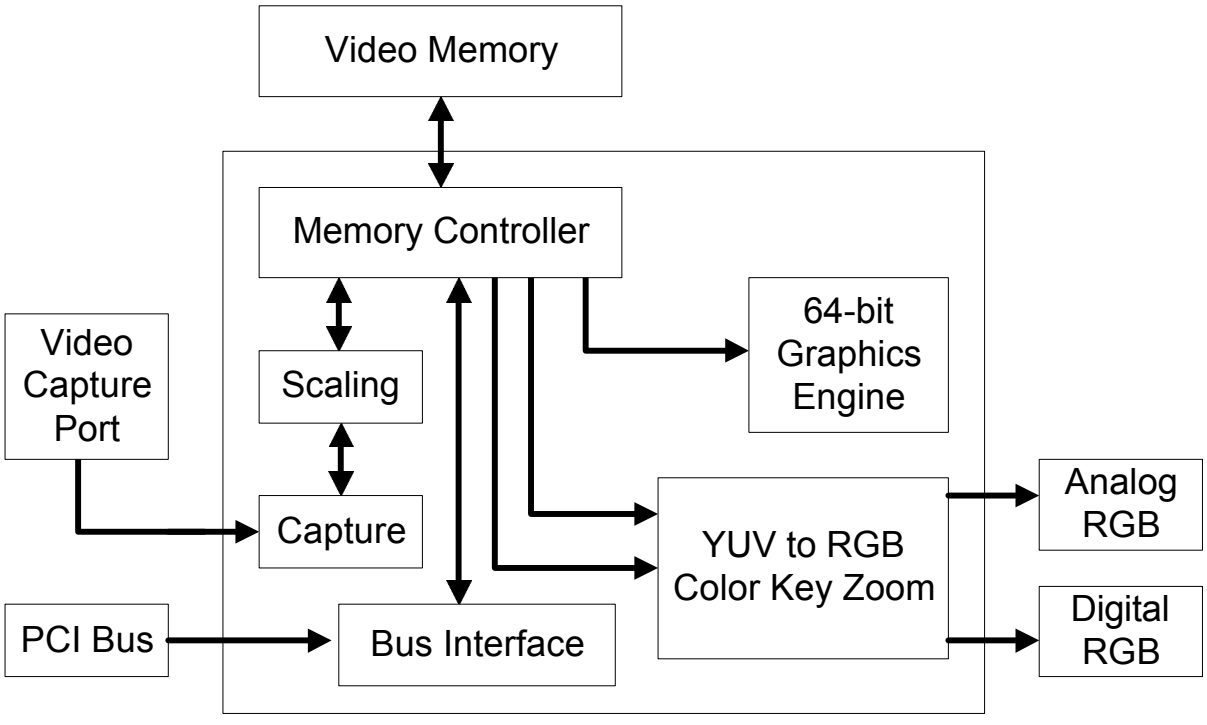


Figure 2-9 C&T 65550 Block Diagram

2.5.3 Pin Diagram

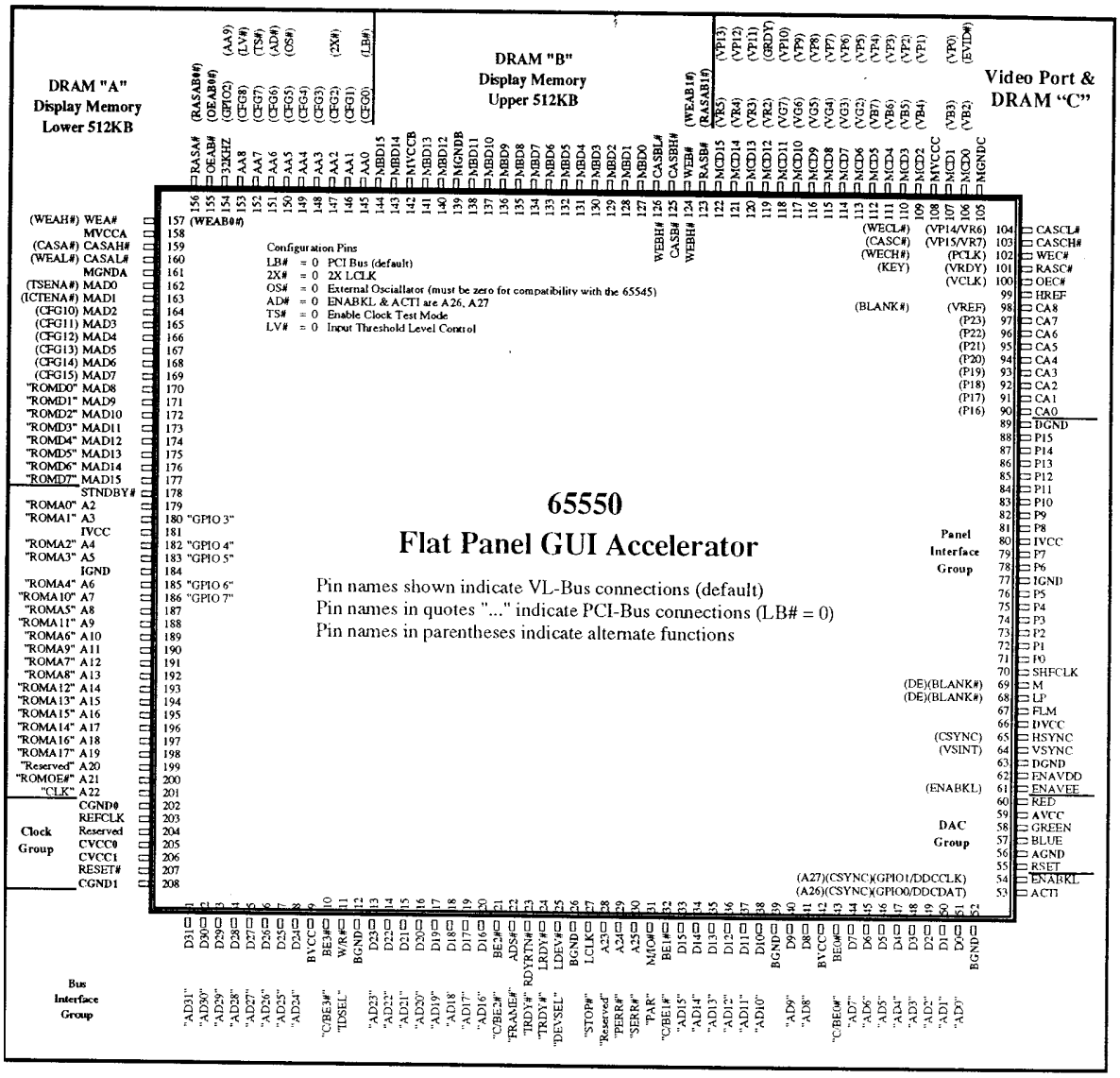


Figure 2-10 C&T 65550 Pin Diagram

2.5.4 Pin Descriptions

Table 2-10 C&T 65550 Pin Descriptions

Pin#	Pin Name	Type	Description
CPU Direct / VL-Bus Interface			
207	RESET	In	Reset. For VL-Bus interfaces, connect to RESET#. For direct CPU local bus interfaces, connect to the system reset generated by the mother board system logic for all peripherals (not the RESET# pin of the processor). This input is ignored during Standby mode (STNDIBY# pin low) so that the remainder of the system (and the system bus) may be safely powered down during Standby mode if desired.
22	ADS#	In	Address Strobe. In VL-Bus and CPU local bus interfaces ADS# indicates valid address and control signal information is present. It is used for all decodes and to indicate the start of a bus cycle.
31	M/IO#	In	Memory /IO. In VL-Bus and CPU local bus interfaces M/IO# indicates either a memory or an I/O cycle: 1 = memory, 0 = I/O
11	W/R#	In	Write / Read. This control signal indicates a write (high) or read (low) operation. It is sampled on the rising edge of the (internal) 1x CPU clock when ADS# is active.
23	RDYRTN# for 1x Clock config CRESET for 2x Clock config	In	Ready Return. Handshaking signal in VL-Bus interface indicating synchronization of RDY# by the local bus master / controller to the processor. Upon receipt of this LCLK-synchronous signal the chip will stop driving the bus (if a read cycle was active) and terminate the current cycle.
24	LRDY#	Out/ OC	Local Ready. Driven low during VL-Bus and CPU local bus cycles to indicate the current cycle should be completed This signal is driven high at the end of the cycle, then tri-stated. This pin is tri-stated during Standby mode (as are all other bus interface outputs).
25	LDEV#	Out	Local Device. In VL Bus and CPU local bus interfaces. this pin indicates that the chip owns the current cycle based on the memory or I/O address which has been broadcast. For VL-Bus, it is a direct output reflecting a straight address decode. This pin is tri-stated during Standby mode (as are all other bus interface outputs).
27	LCLK	In	Local Clock. In VL Bus this pin is connected to the CPU 1x clock. In CPU local bus interfaces it is connected to the CPU 1x or 2x clock. If the input is a 2x clock, the processor reset signal must be connected to CRESET (pin 23) for synchronization of the clock phase.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
CPU Direct / VL-Bus Interface (continued)			
43	BE0# (BLE#)	In	Byte Enable 0. Indicates data transfer on D7:D0 for the current cycle.
32	BE1#	In	Byte Enable 1. Indicates data transfer on D15:D8 for the current cycle.
21	BE2#	In	Byte Enable 2. Indicates data transfer on D23:D16 for the current cycle.
10	BE3#	In	Byte Enable 3. BE3# indicates that data will transfer over the data bus on D31 :24 during the current access.
179 180 182 183 185 186 187 188 189 190 191 192 193 194 195 196 197 189 199 200 201 28 29 30 53 54	A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27	In In In In In In In In In In In In In In In In In In In In In In In In In In	System Address Bus. In VL-Bus, and direct CPU interfaces, the address pins are connected directly to the bus. In internal clock synthesizer test mode (TS# = 0 at Reset), A24 becomes VCLK out and A25 becomes MCLK out. A26 and A27 may be alternately used as General Purpose I/O pins or as Activity Indicator and Enable Backlight respectively (see panel interface pin descriptions, and FROF and FROC for more details). If A26 and A27, are used as GPIO pins, they may be programmed as a 2-pin CRT Monitor DDC interface (VESA™ "Display Data Channel" also referred to as the "Monitor Plug-n-Play" interface). Either A26 or A27 may also be used to output, Composite Sync for support of an external NTSC / PAL encoder chip.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
CPU Direct / VL-Bus Interface (continued)			
51 50 49 48 47 46 45 44 41 40 38 37 36 35 34 33 20 19 18 17 16 15 14 13 8 7 6 5 4 3 2 1	D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24 D25 D26 D27 D28 D29 D30 D31	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	System Data Bus. In 32-bit CPU Local Bus designs these data lines connect directly to the processor data lines. On the VL-Bus they connect to the corresponding buffered or unbuffered data signal. These pins are tri-stated during Standby mode (as are all other bus interface outputs).
PCI Bus Interface			
207	RESET#	In	Reset. This input sets all signals and registers in the chip to a known state. All outputs from the chip are tri-stated or driven to an inactive state. This pin is ignored during Standby mode (STNDBY# pin low). The remainder of the system (therefore the system bus) may be powered down if desired (all bus output pins are tri-stated in Standby mode).
201	CLK	In	Bus Clock. This input provides the timing reference for all bus transactions. All bus inputs except RESET# and INTA# are sampled on the rising edge of CLK. CLK may be any frequency from DC to 33MHz.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
PCI Bus Interface (continued)			
31	PAR	I/O	Parity. This signal is used to maintain even parity across AD0-31 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase (i.e., PAR has the same timing as AD0-31 but delayed by one clock). The bus master drives PAR for address and write data phases; the target drives PAR for read data phases.
22	FRAME#	In	Cycle Frame. Driven by the current master to indicate the beginning and duration of an access. Assertion indicates a bus transaction is beginning (while asserted, data transfers continue); de-assertion indicates the transaction is in the final data phase.
23	IRDY#	In	Initiator Ready. Indicates the bus master's ability to complete the current data phase of the transaction. During a write, IRDY# indicates valid data is present on AD0-31; during a read it indicates the master is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled then asserted (wait cycles are inserted until this occurs).
24	TRDY#	S/TS	Target Ready. Indicates the target's ability to complete the current data phase of the transaction. During a read, TRDY# indicates that valid data is present on AD0-31; during a write it indicates the target is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled then asserted (wait cycles are inserted until this occurs).
27	STOP#	S/TS	Stop. Indicates the current target is requesting the master to stop the current transaction
25	DEVSEL#	S/TS	Device Select. Indicates the current target has decoded its address as the target of the current access
29	PERR# (VCLKOUT)	S/TS	Parity Error. This signal reports data parity errors (except the Special Cycles where SERR# is used). The PERR# is Sustained Tri-state. The receiving agent will drive PERR# active two clocks after detecting a data parity error. PERR# will be driven high for one clock before being tri-stated as with all sustained tri-state signals. PERR# will not report status until the chip has claimed the access by asserting DEVSEL# and completing the data phase.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
PCI Bus Interface (continued)			
30	SERR# (MCLKOUT)	OD	System Error. Used to report system errors where the result will be catastrophic (address parity error, data parity errors for Special Cycle commands, etc.). This output is actively driven for a single PCI clock cycle synchronous to CLK and meets the same setup and hold time requirements as all other bused signals. SERR# is not driven high by the chip after being asserted, but is pulled high only by a weak pull-up provided by the system. Thus, SERR# on the PCI Bus may take two or three clock periods to fully return to an inactive state.
179 180 189 183 185 187 189 191 193 180 188 193 194 196 197 198	ROMA0 ROMA1(GPIO3) ROMA2(GPIO4) ROMA3(GPIO5) ROMA4(GPIO6) ROMA5 ROMA6 ROMA7 ROMA8 ROMA10(GPIO7) ROMA11 ROMA12 ROMA13 ROMA14 ROMA16 ROMA17	Out Out Out Out Out Out Out Out Out Out Out Out Out Out Out Out	BIOS ROM Address Outputs. See MAD8-15 (pins 170-177) for BIOS ROM data inputs. BIOS ROMs are not normally required in portable computer designs (Graphics System BIOS code is normally included in the System BIOS ROM). However, the 65550 provides BIOS ROM interface capability for development systems and add-in card Flat Panel Graphics Controllers. Since the PCI Bus specifications require only one load on the bus for the entire graphics subsystem, the BIOS ROM interface is through the chip. In the VL-Bus mode. the BIOS ROM interface can be an external circuit on the ISA Bus connector that does not require pins on the chip.
200	ROMOE#	Out	BIOS ROM Output Enable.
199	Reserved	In	This pin is always an input (A20 for VL-Bus, reserved for future use on PCI Bus). To avoid abnormal Vcc current due to a floating input for a PCI Bus, use a 10K resistor to ground to pull this pin low..
28	Reserved	In	This pin is always an input (A23 for VL-Bus, reserved for future use on PCI Bus). To avoid abnormal Vcc current due to a floating input for a PCI Bus, use a l0K resistor to ground to pull this pin low.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
PCI Bus Interface (continued)			
51	AD00	I/O	PCI Address / Data Bus. Address and data are multiplexed on the same pins. A bus transaction consists of an address phase followed by one or more data phases (both read and write bursts are allowed by the bus definition). The address phase is the clock cycle in which FRAME# is asserted (AD0-31 contain a 32-bit physical address). For I/O, the address is a byte address; for memory and configuration, the address is a DWORD address. During data phases AD0-7 contain the LSB and 24-31 contain the MSB. Write data is stable and valid when IRDY# is asserted; read data is stable and valid when TRDY# is asserted. Data transfers only during those clocks when both IRDY# and TRDY# are asserted.
50	AD01	I/O	
49	AD02	I/O	
48	AD03	I/O	
47	AD04	I/O	
46	AD05	I/O	
45	AD06	I/O	
44	AD07	I/O	
41	AD08	I/O	
40	AD09	I/O	
38	AD10	I/O	
37	AD11	I/O	
36	AD12	I/O	
35	AD13	I/O	
34	AD14	I/O	
33	AD15	I/O	
20	AD16	I/O	
19	AD17	I/O	
18	AD18	I/O	
17	AD19	I/O	
16	AD20	I/O	
15	AD21	I/O	
14	AD22	I/O	
13	AD23	I/O	
8	AD24	I/O	
7	AD25	I/O	
6	AD26	I/O	
5	AD27	I/O	
4	AD28	I/O	
3	AD29	I/O	
2	AD30	I/O	
1	AD31	I/O	

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
PCI Bus Interface (continued)			
43 32 21 10	C/BE0# C/BE1# C/BE2# C/BE3#	In In In In	Bus Command / Byte Enables. During the address phase. of a bus transaction, these pins define the bus command see list below: C/BE3-0 Command Type 65550 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read Y 0011 I/O Write Y 0100 -reserved- 0101 -reserved- 0110 Memory Read Y 0111 Memory Write Y 1000 -reserved- 1001 -reserved- 1010 Configuration Read Y 1011 Configuration Write Y 1100 Memory Read Multiple 1101 Dual Address Cycle 1110 Memory Read Line 1111 Memory Read & Invalidate During the data phase, these pins are byte enables that determine which byte lanes carry meaningful data: byte 0 corresponds to AD0-7, byte 1 corresponds to 8-15, byte 2 corresponds to 16-23, byte 3 corresponds to 24-31
11	IDSEL		Initialization. Device Select. Used as a chip select during configuration read and write transactions.
145 146 147 148 149 150 151 152 153	AA0 AA1 AA2 AA3 AA4 AA5 AA6 AA7 AA8	I/O I/O I/O I/O I/O I/O I/O I/O I/O	Address bus for DRAMs A and B.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
PCI Bus Interface (continued)			
90 91 92 93 94 95 96 97 98	CA0 (P16) CA1 (P17) CA2 (P18) CA3 (P19) CA4 (P10) CA5 (P21) CA6 (P22) CA7 (P23) CA8 (BLANK)	Out Out Out Out Out Out Out Out I/O	Address bus for DRAM C. CA0-7 may be configured as flat panel data output (P16-23). See also pins 71-88 (in Flat Panel Display interface pin descriptions section). CA8 may be configured as VAFC BLANK# out or vertical reference input (VREF) for video capture.
99	HREF	In	Horizontal reference input for video capture.
156	RASA# (RASAB0#)	Out	RAS for DRAM A (or bank 0 in 2MB configurations)
123	RASB# (RASAB1#)	Out	RAS for DRAM B (or bank 1 in 2MB configurations)
101	RASC# (VRDY) (KEY)	Out In	RAS for DRAM C (or color key input from external PC-Video source or VAFC "Video System Ready" input)
160	CASAL#	Out	CAS for the DRAM A lower byte
159	CASAH#	Out	CAS for the DRAM A upper byte
126	CASBL#	Out	CAS for the DRAM B lower byte
125	CASBH#	Out	CAS for the DRAM B upper byte
104	CASCL# (WECL#) (VR6/VP14)	I/O	DRAM C low byte CAS (or video in red-6 or VAFC VP14)
103	CASCH# (CASC#) (VR7/VP15)	I/O	DRAM C high byte CAS (or video in red-7 or VAFC VP15)
157	WEA# (WEAH#) (WEAB0#)	Out	Write enable for DRAM A (or bank 0 in 2MB)
124	WEB# (WEBH#) (WEAB1#)	Out	Write enable for DRAM B (or bank 1 in 2MB)
102	WEC# (WECH#) (PCLK)	Out	Write enable for DRAM C (or video in port PCLK out)
155	OEAB0#	Out	Output enable for DRAMs A and B, bank 0, 1 of 2MB
100	OEC# (VCLK)	Out In	Output enable for DRAM C (or VAFC "Video Input Clock" if DRAM C not used)

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
Display Memory Interface			
162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177	MAD0 MAD1 MAD2 (CFG10) MAD3 (CFG11) MAD4 (CFG12) MAD5 (CFG13) MAD6 (CFG14) MAD7 (CFG15) MAD8 (PCI ROMD0) MAD9 (PCI ROMD1) MAD10 (PCI ROMD2) MAD11 (PCI ROMD3) MAD12 (PCI ROMD4) MAD13 (PCI ROMD5) MAD14 (PCI ROMD6) MAD15 (PCI ROMD7)	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Memory data bus for DRAM A. (lower 512KB of display memory) MAD2-7 are latched into XR71 register on reset for use as additional configuration inputs (CFG10-12 are reserved by software for input of panel ID). These bits have no other internal hardware configuration function. PCI Bus: MAD8-15 are used as BIOS ROM Data inputs during system startup (i.e., before the system enables the graphics controller memory interface). See also pins 179-199 (in PCI Bus interface pin descriptions section) for BIOS ROM address and ROAM Chip Select outputs. In the VL-Bus mode, the BIOS ROM interface can be an external circuit on the ISA Bus connector.
127 128 129 130 131 132 133 134 135 136 137 138 140 141 143 144	MBD0 MBD1 MBD2 MBD3 MBD4 MBDS MBD6 MBD7 MBD8 MBD9 MBD10 MBD11 MBD12 MBD13 MBD14 MBD15	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Memory data bus for DRAM B (upper 512KB)
106 107 109 110 111 112 113 114 115 116 117 118 119 120 121 122	MCD0 (VB2) (EVID#) MCDI (VB3) (VP0) MCD2 (VB4) (VP1) MCD3 (VB5) (VP2) MCD4 (VB6) (VP3) MCD5 (VB7) (VP4) MCD6 (VG2) (VP5) MCD7 (VG3) (VP6) MCD8 (VG4) (VP7) MCD9 (VG5) (VP8) MCD10 (VG6) (VP9) MCD11(VG7) (VP10) MCD12(VR2) (GRDY) MCD13(VR3) (VP11) MCD14(VR4) (VP12) MCD15 (VR5) (VP13)		Memory data bus for DRAM C (Frame Buffer). When a frame buffer DRAM is not required, this bus may be used to input up to 18 bits of RGB data from an external PC-Video subsystem or 16 bits of RGB from an external VAFC interface. Note that this configuration also provides additional panel outputs so that a video input port may be implemented along with a 24-bit true-color TFT panel (TFT panels never need DRAMC). In VAFC interface mode, pin 106 is the VAFC "Enable Video" Input. The external VAFC interface drives this pin low to indicate data input on the VP0-15. EVID# is ignored (essentially reserved) in the 65550 (VAFC data is always expected as inputs). In VAFC mode, pin 119 is "Graphics System Ready" out and is always driven high.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
Flat Panel Display Interface			
71 72 73 74 75 76 78 79 81 82 83 84 85 86 87 88	P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15	Out Out Out Out Out Out Out Out Out Out Out Out Out Out Out Out	8, 9, 12, or 16-bit flat panel data output. 18-bit and 24-bit panel interfaces may also be supported (see CA0-7 for P16-23). Refer to Table 2-7 for the configurations for various panel types.
70	SHFCLK	Out	Shift Clock. Pixel clock for flat panel data.
67	FLM	Out	First Line Marker. Flat Panel equivalent of VSYNC.
68	LP	Out	Latch Pulse. Flat Panel equivalent of HSYNC.
69	M (DE) (BLANK#)	Out	M signal for panel AC drive control. (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels.
62 61	ENAVDD ENAVEE (ENABKL)	I/O I/O	Power sequencing controls. Power sequencing controls. for panel driver electronics voltage VDD and panel LCD bias voltage VEE
53	ACTI	I/O	Activity Indicator. May be configured for other functions
54	ENBKL	I/O	Enable Backlight Outputs. May be configured for other functions
Flat Panel Display Interface			
65	HYSNC (CSYNC)	Out	CRT Horizontal Sync (polarity is programmable) or "Composite Sync" for support of various external NTSC / PAL encoder chips. Note CSYNC can be set to output on the ACTI or ENABKL pins.
64	VSYNC (VISINT)	Out	CRT Vertical Sync (polarity is programmable) or "Vsync Interval" for support of various external NTSC / PAL encoder chips.
60 58 57	RED GREEN BLUE	Out	CRT analog video outputs from the internal color palette DAC. The DAC is designed for a 37.5 Ω equivalent load on each pin (e.g. 75 Ω resistor on the board, in parallel with the 75 Ω CRT load.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
Flat Panel Display Interface (continued)			
55	RSET	In	Set point resistor for the internal color palette DAC. A 560 Ω 1% resistor is required between RSET and AGND.
59 56	AVCC AGND	VCC GND	Analog power and ground pins for noise isolation for the internal color palette DAC. AVCC should be isolated from digital VCC as described in the Functional Description of the internal color palette DAC. For proper DAC operation, AVCC should not be greater than IVCC. AGND should be common with digital ground but must be tightly decoupled to AVCC. See the Functional Description of the internal color palette DAC for further information .
203	XTALI (MCLK)	In	Crystal In. This pin .serves as the input for an external reference oscillator (usually 14.31818 MHz). Note that in test mode for the internal clock synthesizer, MCLK is output on A25 (pin 30) and VCLK is output on A24 (pin
204	(Reserved)		Reserved. For compatibility with the 65545, this pin (formerly "Crystal Out" or "XTLAO") must be disconnected. In addition, pin 150 must be pulled down on reset. The 65545 no longer supports the "internal oscillator option.
205 202 206 208	CVCC0 CGND0 CVCCI CGNDI	VCC GND VCC GND	Analog power and ground pins for noise isolation for the internal clock synthesizer. Must be the same as VCC for internal logic. VCC/GND pair 0 and VCC/GND pair 1 pins must be carefully decoupled individually. Note that the CVCC voltage must be the same as the voltage for the internal logic (IVCC).
154	32KHz (GP102) (AA9)	In	Clock input for refresh of non-self-refresh DRAMs and panel power sequencing. This pin can be programmed as GP102 instead of 32KHz input, or AA9 for 512Kx3 memory configurations.
Power / Ground and Standby Control			
178	STNDBY#	IN	Standby Control Pin. Pull this pin to place the chip in Standby Mode.
80 77 181 184	IVCC IGND IVCC IGND	VCC GND VCC GND	Power / Ground (Internal Logic). 5V±10% or 3.3V±0.3V. Note that this voltage must be the same as CVCC (voltage for internal clock synthesizer). This voltage must also be equal to, or greater than AVCC (voltage for DAC).
9 12 26 42 39 52	BVCC BGND BGND BVCC BGND BGND	VCC GND GND VCC GND GND	Power / Ground (Bus Interface) 5V±10% or 3.3V±0.3V.

Table 2-10 C&T 65550 Pin Descriptions (continued)

Pin#	Pin Name	Type	Description
Power / Ground and Standby Control (continued)			
66 63 89	DCC DGND DGND	VCC GND GND	Power / Ground (Bus Interface) 5V±10% or 3.3V±0.3V.
158 161 142 139 108 105	MVCCA MGNDA MVCCB MGNDB MVCCC MGNDC		Power / Ground (Bus Interface) 5V±10% or 3.3V±0.3V.

FLAT PANEL DISPLAY INTERFACE (CONFIGURATION BY PANEL TYPES)

Table 2-11 Flat Panel Display Interface Configurations

65550		Mono SS	Mono DD	Mono DD	Color TFT	Color TFT	Color TFT HR	Color STN STN SS	Color STN SS	Color STN DD	Color STN DD	Color STN DD
Pin#	Pin Name	8-bit	8-bit	16-bit	9/12/16 bit	18/24 bit	18/24 bit	8-bit (X4bP)	16-bit (4bP)	8-bit (4bP)	16-bit (4bP)	24 bit
71	P0	-	UD3	UD7	B0	B0	B00	R1	R1	UR1	UR0	UR0
72	P1	-	UD2	UD6	B1	B1	B01	B1	G1	UG1	UG0	UG0
73	P2	-	UD1	UD5	B2	B2	B02	G2	B1	UB1	UB0	UB0
74	P3	-	UD0	UD4	B3	B3	B03	R3	R2	UR2	UR1	LR0
75	P4	-	LD3	UD3	B4	B4	B10	B3	G2	LR1	LR0	LG0
76	P5	-	LD2	UD2	G0	B5	B11	G4	B2	LG1	LG0	LB0
78	P6	-	LD1	UD1	G1	B6	B12	R5	R3	LB1	LB0	UR1
79	P7	-	LD0	UD0	G2	B7	B13	B5	G3	LR2	LR1	UG1
81	P8	P0	-	LD7	G3	G0	G00	SHFCLKU	B3	-	UG1	UB1
82	P9	P1	-	LD6	G4	G1	G01	-	R4	-	UB1	LR1
83	P10	P2	-	LD5	G5	G2	G02	-	G4	-	UR2	LG1
84	P11	P3	-	LD4	R0	G3	G03	-	B4	-	UG2	LB1
85	P12	P4	-	LD3	R1	G4	G10	-	R5	-	LG1	UR2
86	P13	P5	-	LD2	R2	G5	G11	-	G5	-	LB1	UG2
87	P14	P6	-	LD1	R3	G6	G12	-	B5	-	LR2	UB2
88	P15	P7	-	LD0	R4	G7	G13	-	R6	-	LG2	LR2
90	P16	-	-	-	-	R0	R00	-	-	-	-	LG2
91	P17	-	-	-	-	R1	R01	-	-	-	-	LB2
92	P18	-	-	-	-	R2	R02	-	-	-	-	UR3
93	P19	-	-	-	-	R3	R03	-	-	-	-	UG3
94	P20	-	-	-	-	R4	R10	-	-	-	-	UB3
95	P21	-	-	-	-	R5	R11	-	-	-	-	LR3
96	P22	-	-	-	-	R6	R12	-	-	-	-	LG3
97	P23	-	-	-	-	R7	R13	-	-	-	-	LB3
70	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK
	Pixels / Clock:	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3	8

BUS OUTPUT SIGNAL STATUS DURING STANDBY MODE

Table 2-12 Bus Output Signal Status During Standby Mode

65550 Pin#	Signal Name	Signal Status
53	ACTI / A26	Driven Low
54	EBABKL / A27	Driven Low
24	LRDY# / RDY	Tri-Stated
25	LDEV#	Tri-Stated
51-44, 41-40, 38-33	D0-15	Tri-Stated
20-13, 8-1	D16-31	Tri-Stated

S/TS stands for "Sustained Tri-state". These signals are driven by only one device at a time are driven high for one clock before released, and are not driven for at least one cycle after being released by the previous device. A pull-up provided by the bus controller is used to maintain an inactive level between transactions.

2.6 TI PCI1131 CardBus Controller

2.6.1 Overview

The PCI1131 is a bridge between the PCI local bus and two PC Card sockets supporting both 16-bit and 32-bit CardBus PC Cards, and is compliant with the PCI Local Bus Specification Revision 2.1 and PCMCIA's 1995 PCI Card Standard. The PCI 1131 PC Card interface recognizes and identifies PC Cards installed at power-up, run-time, and switches protocols automatically to accommodate 16-bit and 32-bit cards. Support for new 1 6-bit PC Card features such as multi-function cards, 3.3V cards, and DMA, as well as backward compatibility to the PCMCIA Release 2.1-compliant PC Cards are included in the PCI1131. CardBus cards operating at up to 33MHz and with a 32-bit data path offer higher performance, and the PCI1131 allows applications to take full advantage of this bandwidth. The PCI1131 core is powered at 3.3V to provide low power dissipation, but can independently support either 3.3V or 5V signaling on the PCI and PC Card interfaces.

Host software interacts with the PCI1131 through a variety of internal registers which provide status and control information about the PC Cards currently in use, and the internal operation of the PCI1131 itself. These internal registers are accessed by application software either through the PCI Configuration header, or through E programmable windows mapped into PCI memory or I/O address space. The concept of windows is also user by the PCI1131 to pass cycles between PCI and PC Card address spaces, and host software must program the location and size of these windows when the PCI1131 or PC Card is initialized.

The PCI1131 also communicates via a three-line serial protocol to he TI TPS2206 Dual PCMCIA Power Switch. The TPS2206 switches Vcc and Vpp supply voltage to the two PC Card sockets independently. Host software has indirect control over the TPS2206 by writing to internal PCI1131 registers. In order to prevent damage to low-voltage CardBus PC Cards, the PCI1131 will allow only valid Vcc settings to be applied to such cards.

The TPS2206 is the follow-on device to the TPS2202. The PCI1131 will also interface with the TPS2202.

The PCI1131 can notify the host system via interrupts when an event occurs which requires attention from the host. Such events are either card status change events (CSC) or functional interrupts from a PC Card. CSC events occur within the PCI1131 or at the PC Card interface, and indicate a change in the status of the socket (i.e., card insertion or removal). Functional interrupts are interrupts which originate from the PC Card application itself, and are passed from the card to the host system. Both CSC and functional interrupts may be individual masked and routed to a variety of system interrupts. The PCI1131 can signal the system interrupt controll via PCI-style interrupts, ISA IRQ's, or with the Serialized IRQ protocol.

The following sections describe in greater detail how the PCI1131 interacts at an electrical, protocol, and software level at its PCI, PC Card, TPS2206, and interrupt interfaces

2.6.2 Architecture

The Texas Instruments PCI1131 is a high-performance PCI-to-PC Card controller that supports two independent PC Card sockets compliant with the1995 PC Card Standard. The PCI1131 provides a rich set of features which make it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1995 PC Card Standard retains the 16-bit PC Card specification defined in PCMCIA Release 2.1, and defines the new 32-bit PC Card, called CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1131 supports any combination of 16-bit and CardBus PC Cards in its two sockets powered at 5V or 3.3V as required.

The PCI1131 is compliant with the PCI Local Bus Specification Revision 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bus mastering cycles.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1131 is register compatible with the Intel 82365SL-DF ExCA controller. The PCI1131 internal data-path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent, 32-bit write buffers allow fast posted writes to improve system-bus utilization.

An advanced CMOS process is used to achieve low system power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes allow the host power management system to further reduce power consumption.

All unused PCI1131 pins should be pulled high with 43k ohm pull-up resistors.

2.6.3 Features

- 3.3-V Core Logic With Universal PCI Interface Compatible and 3.3-V or 5-V PCI Signaling Environments
- Supports PCI Local Bus Specification 2.1
- Mix and Match 5W3.3V PC Card16 Cards and 3.3V CardBus Cards
- Supports Two PC Card ™ or CardBus Slots With Hot Insertion and Removal
- 1995 PC Card Standard Compliant
- Advanced Submicron, Low-Power CMOS Technology
- Uses Serial Interface to TI TPS2206A Dual Power Switch
- System Interrupts may be Programmed as PCI-style or ISA IRQ-style Interrupts
- ISA IRQ interrupts may be Serialized onto a Single IRQSER Pin
- Programmable Output Select for CLKRUN#
- Supports Burst Transfers to Maximize Data Through put on the PCI and CardBus Bus

- Packaged in a 208-pin TQFP
- Multi-function PCI Device with Separate Configuration Spaces for each Socket
- Five PCI Memory Windows and Two l/O Windows Available to each PC Card16 Socket
- Two l/O Windows and Two Memory Windows Available to each CardBus socket
- CardBus Memory Windows can be Individually selected prefetchable or non-prefetchable
- ExCA™-Compatible Registers Are Mapped in Memory andfilO Space
- Texas Instruments (TI™) Extension Registers Mapped in the PCI Configuration Space
- Intel™ 82365SL-DF Register Compatible
- Supports 16-bit Distributed DMA on Both PC Card Sockets
- Supports PC/PCI DMA on Both PC Card
- Supports ZOOM Video Mode Sockets
- Supports Ring Indicate

2.6.4 Block Diagram

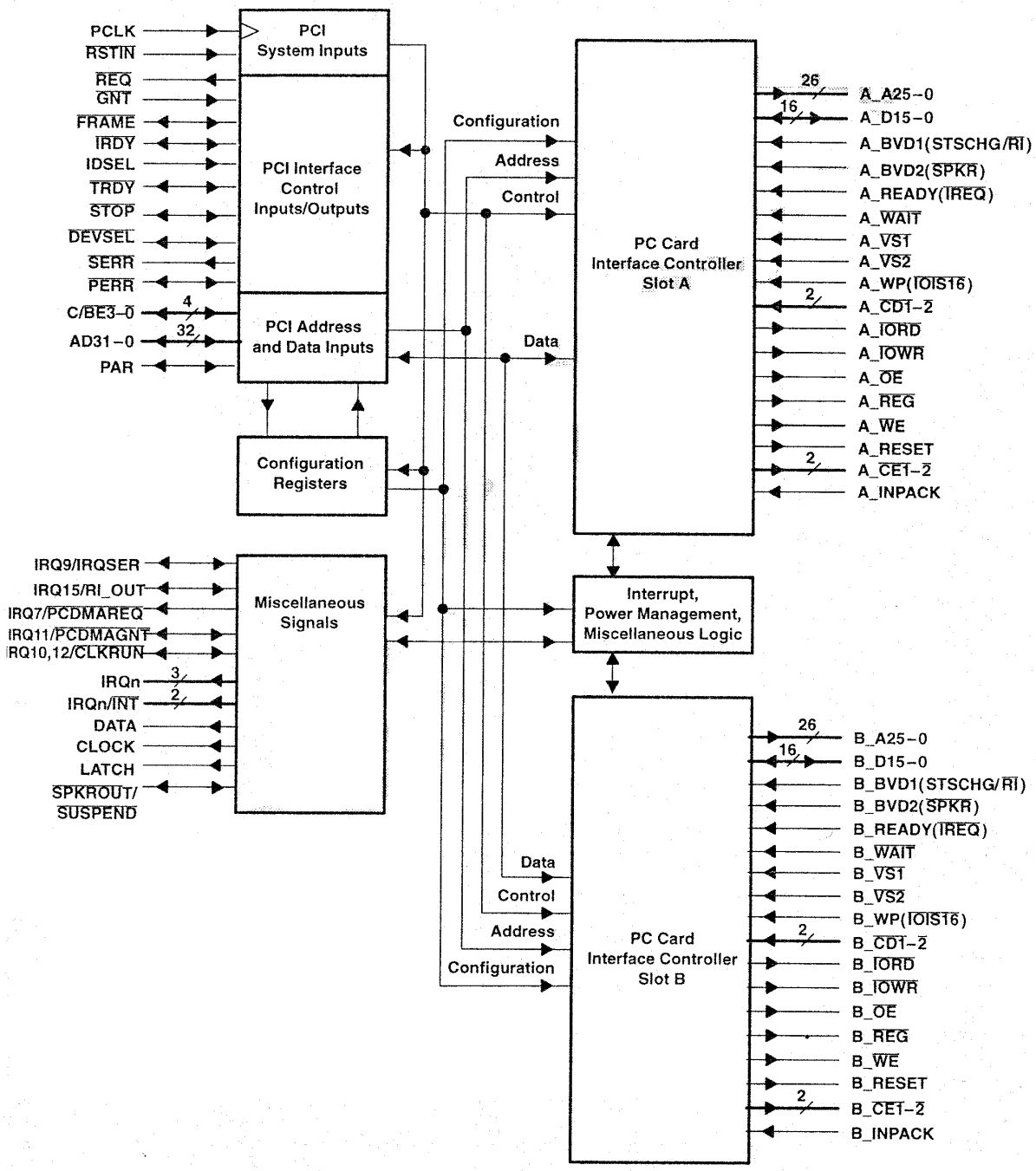


Figure 2-11 Functional Block Diagram - 16-bit PC Card Interface

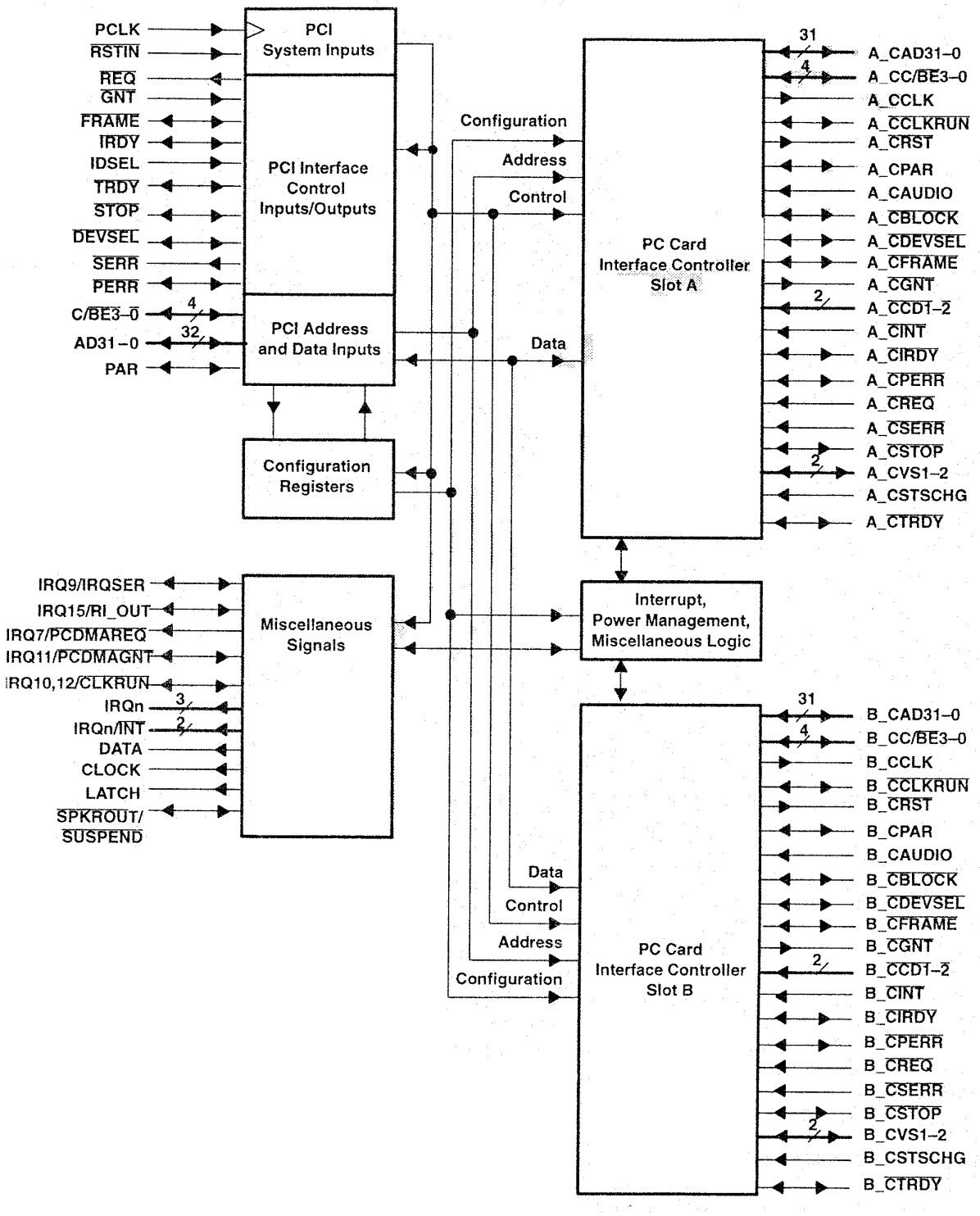


Figure 2-12 Functional block diagram - CardBus Card Interface

2.6.5 Pin Diagram

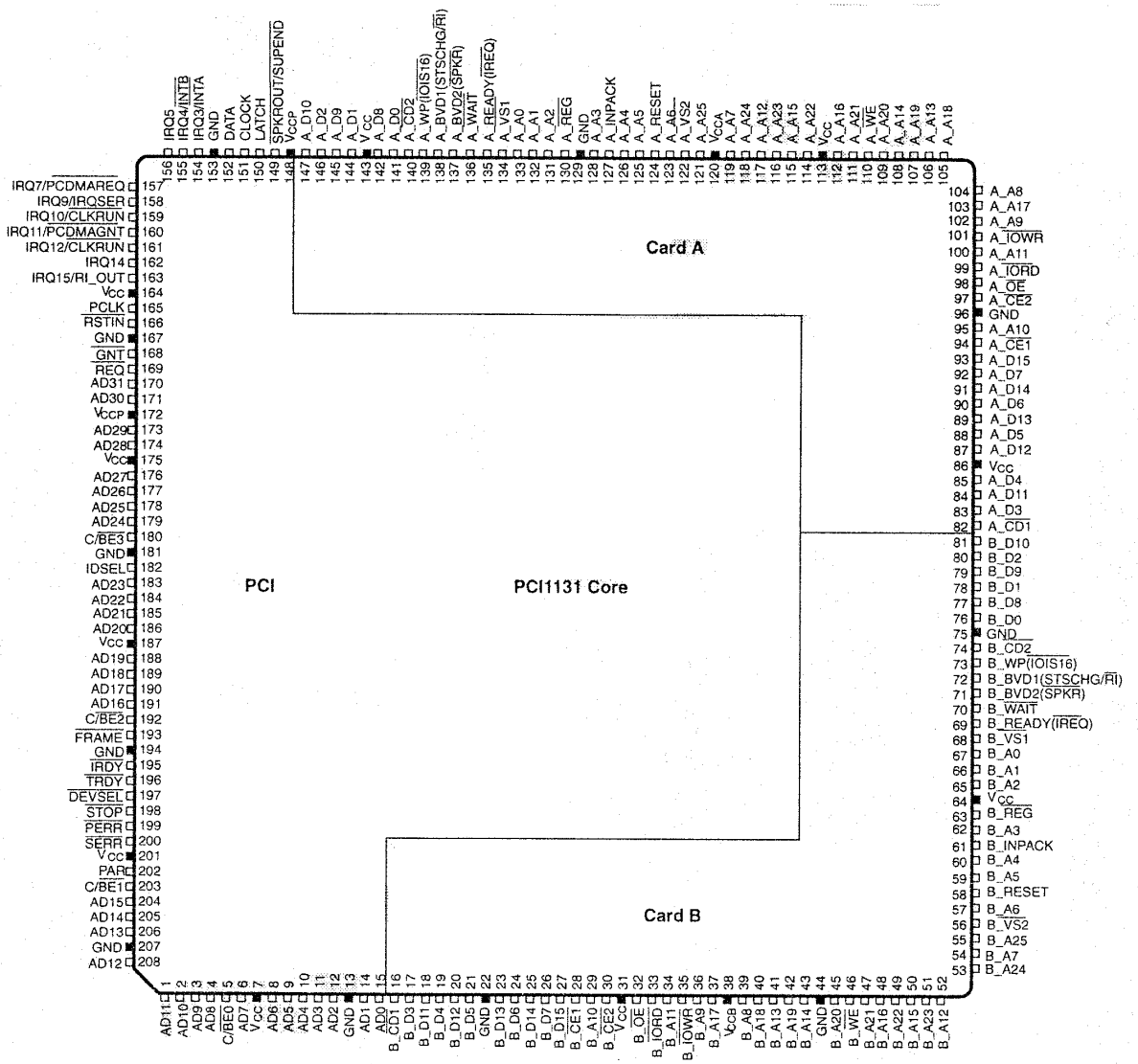


Figure 2-13 PCI-to-PC Card (16-bit) terminal assignments

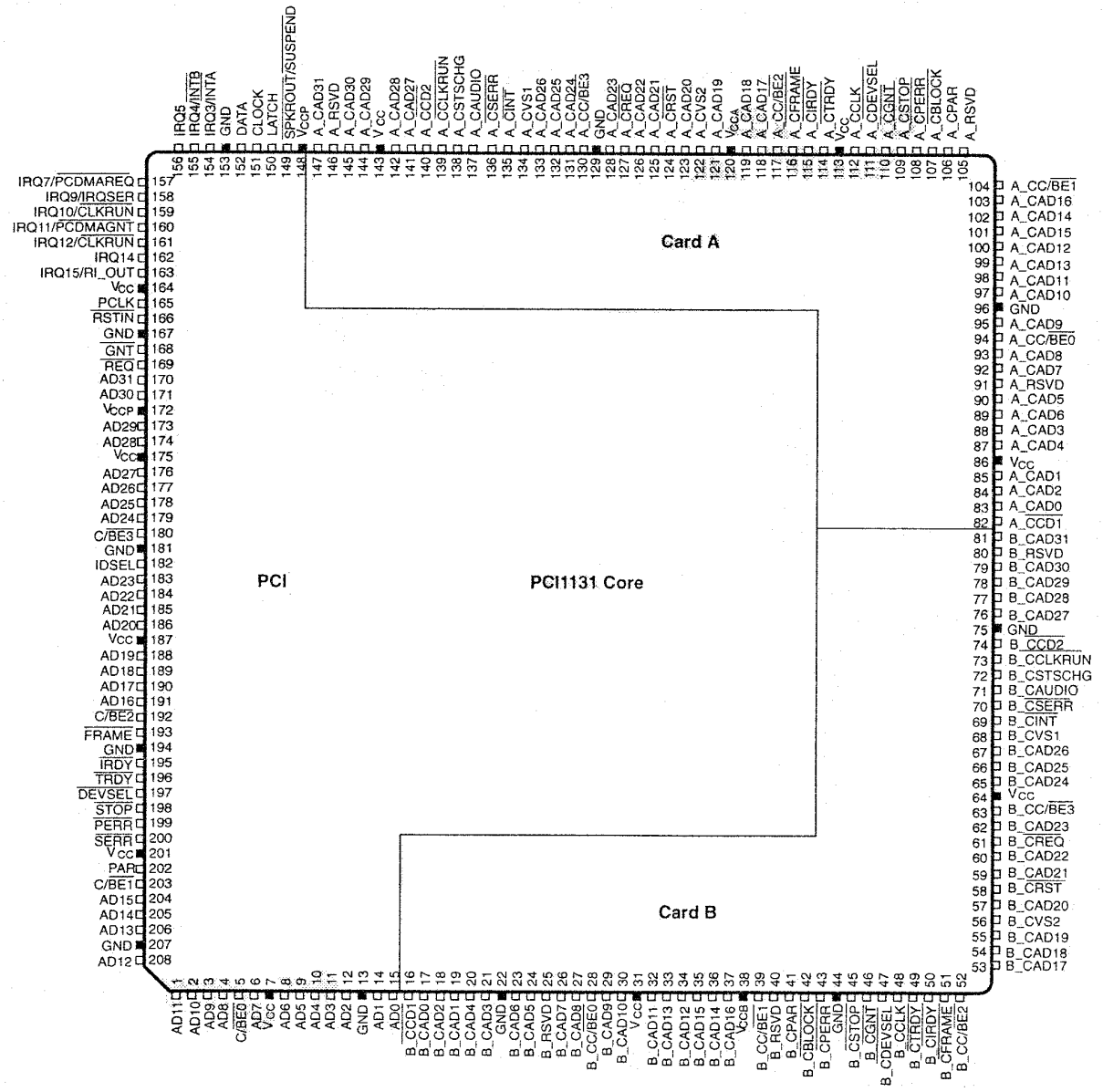


Figure 2-14 PCI-to-CardBus terminal assignments

2.6.6 Terminal Functions

Table 2-13 PCI1131 Pin Descriptions

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
PCI System Terminals			
PCLK	165	I	PCI Bus clock. The PCI bus clock provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
RSTIN	166	I	PCI Reset. When the RSTIN signal is asserted low it causes the PCI1131 to tri-state all output buffers and reset all internal registers. When asserted, the 1131 device is completely nonfunctional. After deasserting RSTIN, the PCI1131 is in its default state. When the 1131 SUSPEND mode is enabled, the device is protected from any RSTIn reset (i.e., the 1131 internal register contents are preserved).
PCI Address and Data Terminals			
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	170 171 173 174 176 177 178 179 183 184 185 186 188 189 190 191 204 205 206 208 1 2 3 4 6 8 9 10 11 12 14 15	I/O	Address/data bus. These signals are the multiplexed PCI address and data bus. During the address phase of a PCI cycle, AD31-0 contain a 32-bits address or other destination information. During the data phase, AD31-0 contain data.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME NO.	I/O TYPE	FUNCTION
PCI Address and Data Terminals		
C/BE3 180 C/BE2 192 C/BE1 203 C/BE0 5	I/O	8us commands and byte enables. These are muitiplexed on the same PCI terminals. During the address phase, C/BE-0 define the bus command. During the data phase, C /ENEW-O are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C/BE0 applies to byte 0 (AD7-0), C/BE1 applies to byte 1 (AD15-8), C/BE2 applies to byte 2 (AD23-16),and C/BE3 applies to byte 3 (AD31-24).
PAR 202	I/O	Parity. As a PCI target during PCI read cycles, or as PCI bus master during PCI write cycles, the PCI 1131 calculates even parity across the AD and C/BE buses and outputs the results on PAR, delayed by one clock.
PCI Interface Control Terminals		
DEVSEL 197	I/O	Device select. As a PCI target, the PCI1131 asserts DEVSEL to claim the current cycle. As a PCI master, the PCI1131 monitors this signal until a target responds or a time out occurs.
FFAME 193		Cycle frame. Driven by the current master to indicate the beginning and duration of an access, FRAME I/O is low (asserted) to indicate that a bus transaction is beginning. While FFGI9IE is asserted, data transfers continue. When FRAME is sampled high (deasserted), the transaction is in the final data phase .
GNT 168	I	Grant. Driven by the PCI arbiter to grant the PCI1131 access to the PCI bus after the current data transaction has completed.
IDSEL 182	I	Initialization device select. IDSEL selects the PCI1t31 during configuration accesses. IDSEL can be connected to one of the upper 24 PCI address lines.
IRDY 195	I/O	Initiator ready. IRDY indicates the bus master's ability to complete the current data phase of the transaction. IRDY is used in conjunction with IRDY. A data phase is completed on any clock where I/O both IRDY and TRDY are sampled low (asserted). During a write, IRDY indicates that valid data is present on AD31-0. During a read, IRDY indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are low (asserted) at the same time. This signal is an output when the PCI1131 is the PCI bos master and an input when the PCI bus target.
STOP 198	I/O	Stop. This signal is driven by the current PCI target to request the master to stop the current transaction.
PERR 99	I/O	Parity error. This signal is driven by the PCI target during a write to indicate that a data parity error has . been detected.
REQ 169	O	Request. Asserted by the PCI1131 to request access to the PCI bus as a master.
SERR 200	O	O System error. Output pulsed from the PCI1131 indicating an address parity error has occurred.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O TYPE	FUNCTION
PCI Interface Control Terminals			
TRDY	196	I/O	Target ready. Indicates the PCI 1131 ability to complete the current data phase of the transaction. TRDY is used in conjunction with IRDY. A data phase is completed on any clock where both TRDY I/O are sampled asserted. During a read, TRDY indicates that valid data is present on AD31-0. During a write, TRDY indicates the PCI1131 is prepared to accept data. Wait cycles are inserted until both TIRDY and TRDY are asserted together. This signal is an output when the PCI 1131 is the PCI target. and an input when it is the PCI bus master.
IRQ10/CLKRUN IRQ12/CLKRUN	159 161	I/O	Interrupt Request 10 and 12. This terminal is software configurable and is used by the PCI 1131 to support the PCI Clock Run protocol. When configured as CLKRUN, by setting bit 0 in the System Control Register at offset 80h, this terminal is an open drain output. To select between IRQ10 and IRQ12 as the output use bit 7 of Register 80h.

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
1 6-bit PC Card Address and Data (Slots A and B)				
A25	121	55	O	PC Card Address. 16-bit PC Card address lines. A25 is the most significant bit.
A24	118	53		
A23	116	51		
A22	114	49		
A21	111	47		
A20	109	45		
A19	107	42		
A18	105	40		
A17	103	37		
A16	112	48		
A15	115	50		
A14	108	43		
A12	106	41		
A11	100	34		
A10	95	29		
A9	102	36		
A8	104	39		
A7	119	54		
A6	123	57		
A5	125	59		
A4	126	60		
A3	128	62		
A2	131	65		
A 1	132	66		
A0	133	67		

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
1 6-bit PC Card Address and Data (Slots A and B)				
D15	93	27	I/O	PC Card Data. 16-bit PC Card data lines. D15 is the most significant bit.
D14	91	25		
D13	89	23		
D12	87	20		
D11	84	18		
D10	147	81		
D9	145	79		
D8	142	77		
D6	90	24		
D5	88	21		
D4	85	19		
D3	83	17		
D2	146	80		
D1	144	78		
D0	141	76		
1 6-bit PC Card Interface Control Signals (Slots A and B)				
CD1	82	16	I	PC Card Detect 1 and Card Detect 2. CD1 and CD2 are connected to ground internally on the PC Card. When a PC Card is inserted into a socket, these signals are pulled low. The signal status is available by reading the Interface Status Register
CD2	140	74		
BVD1 (STSCHG/ RI)	138	72	I	Battery Voltage Detect 1. Generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See the Card Status Change Interrupt Configuration Register for enable bits (Section 8.6). See the Card Status Change Register and the Interface Status Register for the status bits for this signal. Status Change. STSCHG is used to alert the system to a change in the READY, Write Protect, or Battery Voltage Dead condition of a 16-bit I/O PC Card. Ring Indicate. RI is used by 1 6-bit modem cards to indicate ring detection.

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
1 6-bit PC Card Interface Control Signals (Slots A and B)				
BVD2 71 (SPKR)	137		I	Battery Voltage Detect 2. Generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD 1 as an indication of the condition of the batteries on a memory PC Card. Both BVD 1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and needs to be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See the Card Status Change Interrupt Configuration Register for enable bits. See the Card Status Change Register and the Interface Status Register for the status bits for this signal Speaker. SPKR is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I /O interface. The audio signals from cards A and B can be combined by the PCI 1131 and output on SPKROUT. (DMA Request) This pin may be used as the DMA request signal during DMA operations to a 16-bit PC Card which supports DMA. If used, the PC Card asserts this signal to indicate a request for a DMA operation.
REG 63	130		O	Attribute Memory Select. REG remains high for all common memory accesses. When NES is asserted, access is limited to attribute memory (OE or WE active) and to the I /O space (IORD or IOWR active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. (DMA Acknowledge) This pin is used as a DACK during DMA operations to a 1 6-bit PC Card which supports DMA. The PCI 1131 asserts this signal to indicate a DMA operation. This signal is used in conjunction with the DMA Read (IOWR) or DMA Write (IORD) strobes to transfer data.
RESET	124	58	O	PC Card Reset. RESET forces a hard reset to a 16-bit PC Card.
VS1 VS2	134 122	68 56	I/O	Voltage Sense 1 and Voltage Sense 2. VS1 and VS2, when used in conjunction with each other, to determine the operating voltage of the 16-bit PC Card.
INPACK 61	127		I	Input Acknowledge. This signal is asserted by the PC Card when it can respond to an I/O read cycle at the current address. (DMA Request) This pin may be used as the DMA request signal during DMA operations to a 16-bit PC Card which supports DMA. If used, the PC Card asserts this signal to indicate a request for a DMA operation.

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
1 6-bit PC Card Address and Data (Slots A and B)				
IORD	99	33	O	I/O Read. LORD is asserted by the PCI1131 to enable 16-bit I/O PC Card data output during host I/O read cycles. (DMA Write) This pin is used as the DMA write strobe during DMA operations from a 16-bit PC Card which supports DMA. The PCI 1131 asserts this signal during DMA transfers from the PC Card to host memory.
IOWR	101	35	O	I/O Write. IOWR is driven low by the PCI1131 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. (DMA Read) This pin is used as the DMA read strobe during DMA operations to a 16-bit PC Card which supports DMA. The PCI 1131 asserts this signal during DMA transfers from host memory to the PC Card.
OE	98	32	O	Output Enable. OE is driven low by the PCI 1131 to enable 16-bit Memory PC Card data output during host memory read cycles. (DMA Terminal Count) This pin is used as TC during DMA operations to a 16-bit PC Card which supports DMA. The PCI 1131 asserts this signal to indicate Terminal Count for a DMA write operation .
WAIT	136	70	I	Bus Cycle Wait. WET is driven by a 16-bit PC Card to delay the completion of (i e. extend) the memory or I/O cycle that is in progress.
WE	110	46	O	Write Enable . WE is used to strobe memory write data into 16-bit Memory PC Cards. VVE is also used for memory PC Cards that employ programmable memory technologies. (DMA Terminal Count) This pin is used as TC during DMA operations to a 16-bit PC Card which supports DMA. The PCI 1131 asserts this signal to indicate Terminal Count for a DMA read operation.
READY (IREQ)	135	69	I	Ready . The ready function is provided by the READY signal when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit Memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit Memory PC Card is ready to accept a new data transfer. Interrupt Request. IREQ is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I/O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
1 6-bit PC Card Interface Control Signals (Slots A and B)				
WP (IOIS16)	139	73	I	Write Protect. This signal applies to 16-bit Memory PC Cards. WP reflects the status of the write-protect switch on 16-bitmemory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16) function. The status of the signal can be read from the interface status register. (I/O is 16 bits). This signal applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I /O port that is addressed is capable of 16-bit accesses. (DMA Request). This pin may be used as the DMA Request signal during DMA operations to a 16-bit PC Card which supports DMA. If used, the PC Card asserts this signal to indicate a request for a DMA operation.
CE1 CE2	94 97	28 30	O	Card Enable 1 and Card Enable 2. These signals enable even and odd numbered address bytes. CE1 enables even numbered address bytes, and CE2 enables odd numbered address bytes.
CardBus PC Card Address and Data Signals (Slots A and B)				
CAD31 CAD30 CAD29 CAD28 CAD27 CAD26 CAD25 CAD24 CAD23 CAD22 CAD21 CAD19 CAD18 CAD17 CAD16 CAD15 CAD14 CAD13 CAD12 CAD11 CAD10 CAD9 CAD8 CAD7 CAD6 CAD5 CAD4 CAD3 CAD2 CAD1 CAD0	147 145 144 142 141 133 132 131 128 126 123 121 119 118 103 101 102 99 100 98 97 95 93 92 89 90 87 88 84 85 83	81 79 78 77 76 67 66 65 62 60 57 55 54 53 37 35 36 33 34 32 30 29 27 26 23 24 20 21 18 19 17	I/O	CardBus PC Card address and data These pins are multiplexed address and data signals A bus transaction consists of an address phase followed by one or more data phases The PCI 1131 supports both read and write bursts. The address phase is the clock cycle in which CFRAME is asserted. During the address phase, CAD31-0 contain a physical address (32-bits). For I/O, this is a byte address; for configuration and I/O memory, it is a DWORD address. During data phases, CAD74 contain the least significant byte and CAD31-24 contain the most significant byte. Write data is stable and valid when is asserted. Read data is stable and valid when CTRDY is asserted. Data is transferred during those clocks when CIRDY and CTRDY are asserted. ***Note:*** *+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.* ≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
CardBus PC Card Address and Data Signals (Slots A and B)				
CC/BE0 CC/BE1 CC/BE2 CC/BE3	94 104 117 130	28 39 52 63	I/O	CardBus PC Card Command and Byte Enables. These signals are multiplexed on the same pin. During the address phase of the transaction, CC/BE3 0 define the bus command. During the data I/O phase transaction, CC/BE3-0 are used as Byte Enables. Byte Enables are valid during the entire data phase and determine the byte lanes that will carry the data. CC/BE0 applies to byte 0, CC/BE3 applies to byte 1, CC/EE2 applies to byte 2, and CC/BE3 applies to byte 3.
CPAR	106	41	I/O	CardBus PC Card Parity. Even parity across CAD3 1-0 and CC/ES3-O is calculated and driven by this signal. CPAR is stable and valid for one clock after the address phase. For Data phases, CPAR is stable and valid one clock after either CIRDY is asserted on a write transaction or CTRDY is asserted on a read transaction. Once CPAR is valid, it remains valid for one clock after the completion of the current data phase. Note: CPAR has the same timing as CAD31-0 but delays by one clock. When the PCI 1131 is acting as an initiator, it will drive CPAR for address and write data phases; and when acting as a target, the PCI1131 will drive CPAR for read data phases.
CardBus PC Card Interface System Signals (Slots A and B)				
CCLK	112	48	O	CardBus PC Card Clock. This signal provides synchronous timing for all transactions on the CardBus PC Card interface. All signals except MST (upon assertion) CCLKRUN, CIST, CSTSCHG, CAUDIO, CCD2-1, and CVS2-1 are sampled on the rising edge of the clock, and all timing parameters are defined with the rising edge of this signal. The CardBus clock operates at 33 MHz, but it can be stopped in the low state.
CCLKRUN	139	73	I/O	CardBus PC Card Clock Run. This signal is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI 1131 to indicate that the CCLK frequency will be decreased.
CRST	124	58	O	CardBus PC Card Reset. This signal is used to bring CardBus PC Card specific registers, sequencers, and signals to a consistent state. When ZMT is asserted, all CardBus PC Card signals must be driven to high impedance state, but the PCI 1131 will drive these signals to a valid logic level. Assertion may be asynchronous for the CCLK but deassertion must be synchronous to the CCLK.
CardBus PC Card Interface Control Signals (Slots A and B)				
CCD1 CCD2	82 140	16 74	I	CardBus Detect 1 and CardBus Detect 2. CCD1 and CCD2 are used in conjunction with CVS1 and CVS2 to determine the type and voltage of the CardBus PC Card. The signal status is available by reading the Interface Status Register

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name Slot Slot A+ B≠	I/O TYPE	FUNCTION
CardBus PC Card Interface Control Signals (Slots A and B)		
CBLOCK 107 42	I/O	CardBus Lock. This is an optional signal used to lock a particular address, ensuring a bus initiator exclusive access. NOTE: This signal is not supported on the PCI 1131.
CDEVSEL 111 47	I/O	CardBus Device Select. When actively driven, this signal indicates that the PCI 1131 has decoded its address as the target of the current access. As an input, CDEVSEL indicates whether any device on the bus has been selected.
CDEVSEL 109 45	I/O	CardBus Stop. This signal indicates the current target is requesting the initiator to stop the current transaction.
CSTSCHG 138 72	I	CardBus Status Change. CSTSCHG is used to alert the system to a change in the READY, WP, or BVD condition of the I/O CardBus PC Card.
CAUDIO 137 71	I	CardBus Audio. This signal is an optional digital input signal from a PC Card to the system's speaker. CardBus cards support two types of audio: single amplitude, binary waveform, and/or Pulse Width Modulation (PWM) encoded signal. The PCI1131 supports the Binary Audio Mode, and may output a binary audio signal from the PC Card to the SPKROUT signal.
CIRDY 115 50	I/O	CardBus Initiator Ready. This signal indicates that the PCI1131 is initiating the bus initiator ability to complete a current data phase of the transaction. It is used in conjunction with CTRDY. When both of these signals are sampled asserted, a data phase is completed on any clock. During a write, CIRDY indicates that valid data is present on CAD31-0, and during a read, it indicates the PCI 1131, as an initiator, is prepared to accept the data. Wait cycles are inserted until both CTRDY and CFRDY are both low (asserted).
CTRDY 114 49	I/O	CardBusTargetReady. This signal indicates that the PCI 1131, as a selected targets has the ability to complete a current data phase of the transaction. It is used in conjunction with CIRDY. When both of these signals are sampled asserted, a data phase is completed on any clock. During a read, CTRDY indicates that valid data is present on CAD31-0, and during a write, it indicates the PCI 1131, as a target, is prepared to accept the data. Wait cycles are inserted until both CIRDY and CTRDY are both low (asserted).
CFRAME 116 51	I/O	CardBus Cycle Frame. This signal is driven by the PCI 1131 when it is acting as an initiator to indicate the beginning and duration of a transaction. CFRAME is asserted to indicated a bus transaction is beginning, and while it is asserted, data transfer is continuous. When CFRAME is high (deasserted), the transaction is in its final data phase.

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL Name	Slot A+	Slot B≠	I/O TYPE	FUNCTION
CardBus PC Card Interface Control Signals (Slots A and B)				
CREQ	127	61	I	CardBus Request. This signal ir1dicates to the arbiter that the CardBus PC Card desires use the CardBus bus.
CGNT	110	46	O	CardBus Grant. This signal is driven by the PCI 1131 to grant a CardBus PC Card access to the CardBus bus after the current data transaction has completed
CPERR	108	43	I/O	CardBus Parity Error. This signal reports errors during all CardBus PC Card transactions except during special cycles. This signal is sustained in a high-impedance state and must be driven active by the agent receiving data, two clocks following the data, when a data parity error is detected. This signal must be driven active for a minimum duration is one clock for each data phase. CPERR must be driven high for one clock before it is returned to the high-impedance state. An agent cannot report a CPERR until it has claimed the access by asserting CDSVSEL and completed a data phase.
CSERR	136	70	I	CardBus System Error. This signal reports address parity error, data errors on the Special Cycle command, or any other system error where the result could be catastrophic, such that the CardBus card may no longer operate correctly. CSERR is open drain and is actively driven for a single CardBus PC Card clock by the agent reporting the error. The assertion of this signal is synchronous to the Cock and meets the setup and hold times of all bussed signals. Restoring of the CSERR to the deasserted states is accomplished by a weak pull-up which is provided by the system designer. This pull-up may take two to three clock periods to fully restore ~R The PCI1131 reports CSERR to the operating system anytime it is sampled low (asserted)
CVS1 CVS2	134 122	68 56	I/O	CardBus Voltage Sense 1 and Voltage Sense 2. CVS1 and CVS2, are used in conjunction with each other, along with CCD1 and CCD2, to determine the operating voltage of the CardBus PC Card.
CINT	135	69	I	CardBus Interrupt. This signal is asserted low by a CardBus PC Card to request interrupt servicing from the host.

+ Terminal name is preceded with A_. As an example, the full name for terminal 121 is A_A25.

≠ Terminal name is preceded with B_. As an example, the full name for terminal 55 is B_A25.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME	NO	I /O TYPE	FUNCTION
Interrupt Terminals			
IRQ3/INTA IRQ4/INTB	154 155	O	Interrupt Request 3 and Interrupt Request 4. These terminals may be connected to either PCI or ISA interrupts. These terminals are software configurable as IRQ3 or T1VTA, and as IRQ4 or T1~. When configured for IRQ3 and IRQ4, these terminals should be connected to the ISA IRQ programmable interrupt controller. When these pins are configured for INTA and INTB, these terminals should be connected to available interrupts on the PCI bus.
IRQ7/ PCDMAREQ	157	O	Interrupt Request 7. This terminal is software configurable and is used by the PCI1131 to request PC/PCI DMA transfers from chip sets that support the PC/PCI DMA scheme. When this pin is configured for PC/PCI DMA request (IRQ7) it should be connected to the appropriate request (REQ#) pin on the Intel MPIIX controller.
IRQ9/ IRQSER	158	O	Interrupt Request 9. This terminal is software configurable and indicates an interrupt request from one of the PC Cards. When this pin is configured for IRQ9 it should be connected to the IRQ programmable interrupt controller. IRQSER allows all IRQ signals to be serialized onto one pin. This signal is configured in the Device Control Register of the TI Extension Registers.
IRQ11/ PCDMAGNT	160	O	Interrupt Request 11. This terminals software configurable and is used by the PCI 1131 to accept a grant for PC/PCI DMA transfers from chip sets that support the PC/PCI DMA scheme. When this pin is configured for PC/PCI DMA grant (IRQ11) it should be connected to the appropriate grant (GNT#) pin on the Intel MPIIX controller.
IRQ10/ CLKRUM IRQ12/ CLKRUM	159 161	I/O	Interrupt Request 10 and t2. This terminal is software configurable and is used by the PCI1131 to support the PCI Clock Run protocol. When configured as CLKRUN, by setting bit 0 in the System Control Register at offset 80h (Section 7.27), this terminal is an open drain output. To select between IRQ10 and IRQ12 as the output use bit 7 of Register 80h.
IRQ5 IRQ14	156 162	O	Interrupt Requests 5 and 14. These signals are ISA interrupts. These terminals indicate an interrupt request from one of the PC Cards. The Interrupt mode is selected in the Device Control Register of the TI Extension Registers.

Table 2-13 PCI1131 Pin Descriptions (Continued)

TERMINAL NAME	NO	I /O TYPE	FUNCTION
Interrupt Terminals			
IRQ15/ RI_OUT	163	I/O	Interrupt Request 15. This terminal indicates an interrupt request from one of the PC Cards. RI_OUT allows the RI input from the 1 6-bit PC Card, CSTSCHG from CardBus Cards or PC Card removal events to be output to the system. This signal is configured in the Card Control Register of the TI Extension Registers.
PC Card Power Switch Terminals			
LATCH	150	O	Power Switch Latch is asserted by the PCI1131 to indicate to the PC Card power switch that the data on the DATA line is valid.
CLOCK	151	O	Power Switch Clock. Information on the DATA line is sampled at the rising edge of CLOCK. The frequency of the clock is derived from dividing the PCICLK by 36. The maximum frequency of this signal is 2 MHz.
DATA	152	O	Power Switch Data is used by the PCI1131 to serially communicate socket power control information.
Speaker Control Terminal			
SPKROUT/ SUSPEND	149	I/O	Speaker. SPKROUT carries the digital audio signal from the PC Card. SUSPEND, when enabled, this signal places the PCI1131 in PCI1131 Suspend Mode (Section 6.0) . This pin is configured in the Card Control Register (Section 7.29) of the TI Extension Registers.
Power Supply Terminals			
GND	13,22,44 75 96,129, 153, 167, 81 194,207	I	Device ground terminals
VccA	120	I	Power-supply terminal for PC Card A (5V or 3.3V)
VccB	38	I	Power-supply terminal for PC Card B (5V or 3.3 V)
VccP	148, 172	I	Power-supply terminal for PCI interface (5V or 3.3V)
Vcc	7, 31, 64, 86, 113, 143,164, 175, 187, 201	I	Power-Supply terminal for core logic (3.3V)

2.7 NS87336VJG Super I/O Controller

The PC87336VJG is a single chip solution for most commonly used I/O peripherals in ISA, and EISA based computers. It incorporates a Floppy Disk Controller(FDC), two full featured UARTs, and an IEEE 1284 compatible parallel port Standard PC-AT address decoding for all the peripherals and a set of configuration registers are also implemented in this highly integrated member of the Super I/O family. Advanced power management features, mixed voltage operation and integrated Serial-Infrared(both IrDA and Sharp) support makes the PC87336 an ideal choice for low-power and/or portable personal computer applications.

The PC87336 FDC uses a high performance digital data separator eliminating the need for any external filter components. It is fully compatible with the PC8477 and incorporates a superset of DP8473, NEC PD765 and N82077 floppy disk controller functions. All popular 5.25" and 3.5" floppy drives, including the 2.88 MB 3.5" floppy drive, are supported. In addition, automatic media sense and 2 Mbps tape drive support are provided by the FDC.

The two UARTs are fully NS16450 and NS16550 compatible. Both ports support MIDI baud rates and one port also supports IrDA's the HP SIR and Sharp SIR compliant signaling protocol.

The parallel port is fully IEEE 1284 level 2 compatible. The SPP(Standard Parallel Port) is fully compatible wit ISA and EISA parallel ports. In addition to the SPP, EPP(Enhanced Parallel Port) and ECP(Extended Capabilities Port) modes are supported by the parallel port.

A set of configuration registers are provided to control the Plug and Play and other various functions of the PC87336. These registers are accessed using two 8-bit wide index and data registers. The ISA I/O address of the register pair can be relocated using a power-up strapping option and the software configuration after power-up.

When idle, advanced power management features allows the PC87336 to enter extremely low power modes under software control. The PC87336 can operate from a 5V or a 3.3V power supply. An unique I/O cell structure allows the PC87336 to interface directly with 5V external components while operating from a 3.3V power supply.

2.7.1 Features

- 100% compatible with ISA, and EISA architectures
- The Floppy Disk Controller:
  - Software compatible with the DP8473, the 765A and the N82077
  - 16-byte FIFO(disabled by default)
  - Burst and Non-Burst modes
  - Perpendicular Recording drive support
  - New high-performance internal digital data separator(no external filter components required)
  - Low-power CMOS with enhanced power-down mode
  - Automatic media-sense support, with full IBM TDR(Tape Drive Register) implementation
  - Supports fast 2 Mbps and standard 1 Mbps/500 kbps/250 kbps tape drives

- The Bidirectional Parallel Port:
  - Enhanced Parallel Port(EPP) compatible
  - Extended Capabilities Port(ECP) compatible, including level 2 support
  - Bidirectional under either software or hardware control
  - Compatible with ISA, and EISA, architectures
  - Ability to multiplex FDC signals on parallel port pins allows use of an external Floppy Disk Drive(FDD)
  - Includes protection circuit to prevent damage to the parallel port when a connected printer is powered up or is operated at a higher voltage
- The UARTs:
  - Software compatible with the PC16550A and PC16450
  - MIDI baud rate support
  - Infrared support on UART2(IrDA and Sharp-compliant)
- The Address Decoder
  - 6 bit or 10 bit decoding
  - External Chip Select capability when 10 bit decoding
  - Full relocation capability(No limitation)
- Enhanced Power Management
  - Special configuration registers for power-down
  - Enhanced programmable power-down FDC command
  - Auto power-down and wake-up modes
  - 2 special pins for power management
  - Typical current consumption during power-down is less than 10 uA
  - Reduced pin leakage current
- Mixed Voltage support
  - Supports standard 5V operation
  - Supports 3.3V operation
  - Supports mixed internal 3.3V operation with 3.3V/5V external configuration
- The General Purpose Pins:
  - 2 pins, for 2 separate programmable chip select decoders, can be programmed for game port control

- Plug and Play Compatible:
  - 16 bit addressing(full programmable)
  - 10 selectable IRQs
  - 3 selectable DMA Channels
  - 3 SIRQ Inputs allows external devices to mapping IRQs
- 100-Pin TQFP package - PC87336VJG

2.7.2 Block Diagram

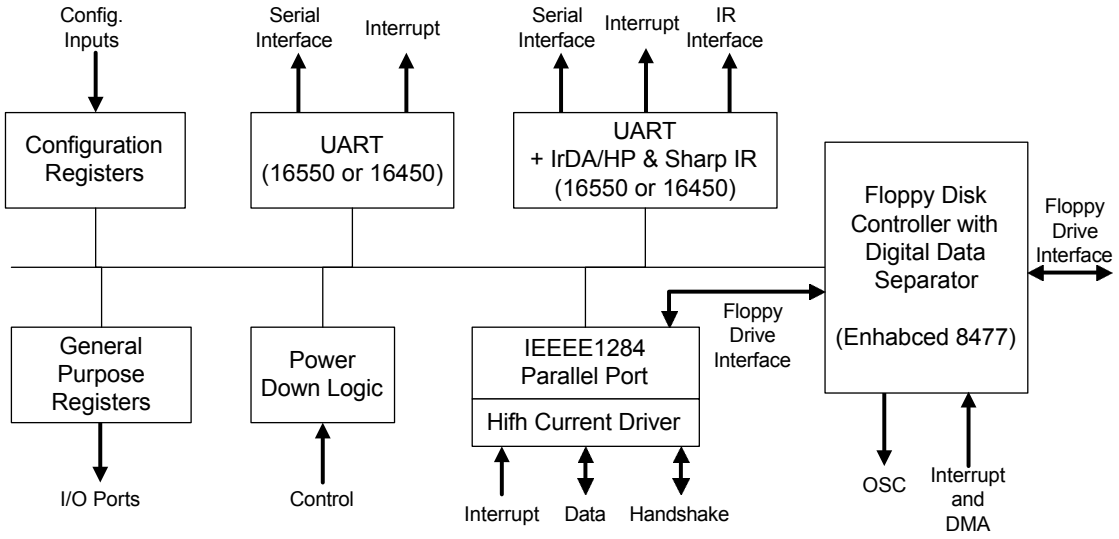


Figure 2-15 NS87336VJG Block Diagram

2.7.3 Pin Diagram

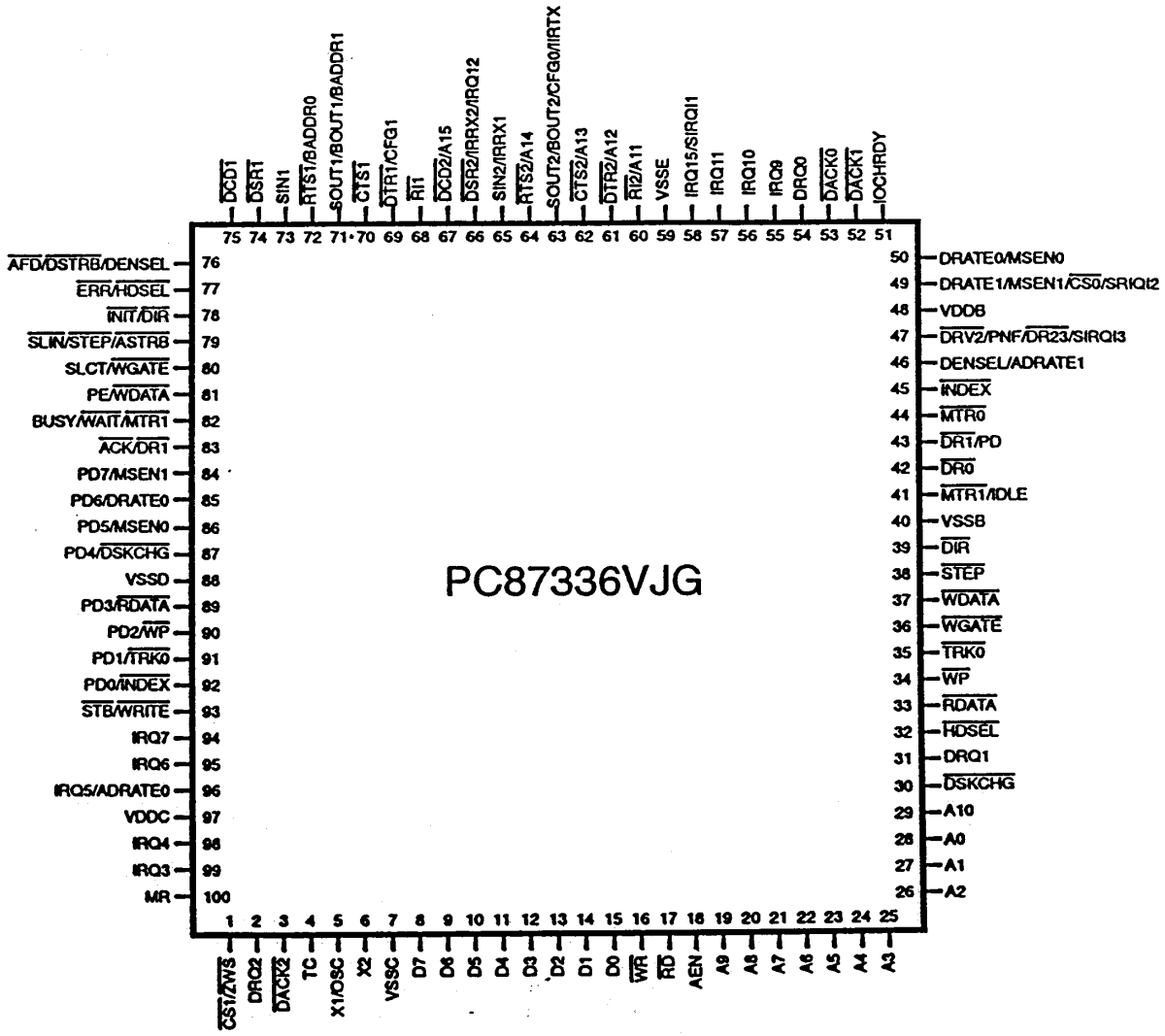


Figure 2-16 NS87336VJG Pin Diagram

2.7.4 Pin Description

Table 2-14 NS87336VJG Pin Descriptions

Pin	No.	I/O	Description
A15-A0	67, 64, 62-60, 29, 19-28	I	Address. These address lines from the microprocessor determine which internal register is accessed. A0-A15 are don't cares during DMA transfer.
/ACK	83	I	Parallel Port Acknowledge. This input is pulsed low by the printer to indicate that it has received the data from the parallel port. This pin has a nominal 25 KΩ pull-up resistor attached to it.
ADRATE0, ADRATE1	96, 46	O	FDD Additional Data Rate 0,1. These outputs are similar to DRATE0, 1. They are provided in addition to DRATE0, 1. They reflect the currently selected FDC data rate, (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). ADRATE0 is configured when bit 0 of ASC is 1. ADRATE1 is configured when bit 4 of ASC is 1. (See IRQ5 and DENSEL for further information).
/AFD	76	I/O	Parallel Port Automatic Feed XT. When this signal is low, the printer automatically line feed after printing each line. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.
AEN	18	I	Address Enable. When this input is high, it disables function selection via A15-A0. Access during DMA transfer is not affected by this pin.
/ASTRB	79	O	EPP Address Strobe. This signal is used in EPP mode as address strobe. It is an active low signal.
BADDR0, BADDR1	72, 71	I	Base Address. These bits determine one of the four base addresses from which the Index and Data Registers are offset. An internal pull-down resistor of 30 KΩ is on this pin. Use a 10 KΩ resistor to pull this pin to VCC.
BOUT1, BOUT2	71, 63	O	UARTs Baud Output. This multi-function pin supports the associated serial channel Baud Rate generator output signal if the test mode is selected in the Power and Test Configuration Register and the DLAB bit (LCR7) is set. After the Master Reset, this pin offers the SOUT function.
BUSY	82	I	Parallel Port Busy. This pin is set high by the printer when it cannot accept another character. It has a nominal 25 KΩ pull-down resistor attached to it.
CFG0 CFG1	63, 69	I	Configuration on Power-up. These CMOS inputs select 1 of 4 default configurations in which the PC87336 powers up. An internal pull-down resistor of 30 KΩ is on each pin. Use a 10 KΩ resistor to pull these pins to VCC.

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
/CS0, /CS1	51, 3	O	Programmable Chip Select. /CS0, 1 are programmable chip select and/or latch enable and/or output enable signals that can be used as game port, I/O expand, etc. The decoded address and the assertion conditions are configured via the 87336VJG's configuration registers.
/CTS1, /CTS2	72, 64	I	UARTs Clear to Send. When low, this indicates that the modem or data set is ready to exchange data. The /CTS signal is a modem status input. The CPU tests the condition of this /CTS signal by reading bit 4 (CTS) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 4 is the complement of the CTS signal. Bit 0 (DCTS) has no effect on the transmitter. /CTS2 is multiplexed with A13. When it is not selected, it is masked to "0". **NOTE:** *Whenever the MSR DCTS bit is set, an interrupt is generated if Modem Status interrupts are enabled.*
D7-D0	10-17	I/O	Data. These are bidirectional data lines to the microprocessor. D0 is the LSB and D7 is the MSB. These signals have a 24 mA (sink) buffered outputs.
/DACK0 /DACK1 /DACK2	53, 52, 3	I	DMA Acknowledge 0, 1, 2. These active low inputs acknowledge the DMA request and enable the /RD and /WR inputs during a DMA transfer. It can be used by one of the following: FDC or Parallel Port. If none of them uses this input pin, it is ignored. If the device which uses on of this pins is disabled or configured with no DMA, this pin is also ignored. /DACK0, 1, 2should be held high during I/O accesses.
/DCD1, /DCD2	75, 67	I	UARTs Data Carrier Detect. When low, this indicates that the modem or data set has detected the data carrier. The /DCD signal is a modem status input. The CPU tests the condition of this /DCD signal by reading bit 7 (DCD) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MSR indicates whether DCD input has changed state since the previous reading of the MSR. **NOTE:** *Whenever the MSR DDCD bit is set, an interrupt is generated if Modem Status interrupts are enabled.*

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
DENSEL (Normal Mode)	46	O	FDC Density Select. DENSEL indicates that a high FDC density data rate (500 Kbs, 1 Mbs or 2 Mbs) or a low density data rate (250 or 300 Kbs) is selected. DENSEL is active high for high density (5.25-inch drives) when IDENT is high, and active low for high density (3.5-inch drives) when IDENT is low. DENSEL is also programmable via the Mode command.
DENSEL (PPM Mode)	76	O	FDC Density Select. This pin offers an additional Density Select signal in PPM Mode when PNF=0.
/DIR (Normal Mode)	39	O	FDC Direction. This output determines the direction of the floppy disk drive (FDD) head movement (active = step-in; inactive = step-out) during a seek operation. During reads or writes, DIR is inactive.
/DIR (PPM Mode)	78	O	FDC Direction. This pin offers an additional Direction signal in PPM Mode when PNF = 0.
/DR0, /DR1 (Normal Mode)	42, 43	O	FDC Drive Select 0, 1. These are the decoded drive select outputs that are controlled by Digital Output Register bits D0, D1. The Drive Select outputs are gated with DOR bits 4-7. These are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. DR0 exchanges logical drive values with DR1 when bit 4 of Function Control Register is set.
/DR1 (PPM Mode)	83	O	FDC Drive Select 1. This pin offers an additional Drive Select signal in PPM Mode when PNF = 0. It is drive select 1 when bit 4 of FCR is 0. It is drive select 0 when bit 4 of FCR is 1. This signal is active low.
/DR23	47	O	FDC Drive 2 or 3. /DR23 is asserted when either Drive 2 or Drive 3 is assessed(except during logical drive exchange).
/DRATE0 /DRATE1 (Normal Mode)	50, 49	O	FDC Data Rate 0, 1. These outputs reflect the currently selected FDC data rate (bits 0 and 1 in the Configuration Control Register (CCR) or the Data Rate Select Register (DSR), whichever was written to last). The pins are totem-pole buffered outputs (6 mA sink, 6 mA source).
/DRATE0 (PPM Mode)	85	O	FDC Data Rate 0. This pin provides an additional Data Rate signal, in PPM mode, When PNF=0.
DRQ0 DRQ1 DRQ2	54 31 2	O	DMA Request 0, 1, 2. \An active high output that signals the DMA controller that a data transfer is required. This DMA request can be sourced by one of the following: FDC or Parallel Port. When it is not sourced by and of them, it is in TRI-STATE. When the sourced device is disabled or when the sourced device is configured with no DMA, it is also in TRI-STATE. Upon reset, DRQ2 is used by the FDC.

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
/DRV2	47	I	FDD Drive2. This input indicates whether a second disk drive has been installed. The state of this pin is available from Status Register A in PS/2 mode. (See PNF for further information).
/DSKCHG (Normal Mode)	30	I	Disk Change. The input indicates if the drive door has been opened. The state of this pin is available from the Digital Input Register. This pin can also be configured as the RGATE data separator diagnostic input via the Mode command.
/DSKCHG (PPM Mode)	87	I	Disk Change. This pin offers an additional Disk Change signal in PPM Mode when PNF = 0.
/DSR1 /DSR2	74, 66	I	UARTs Data Set Ready. When low, this indicates that the data set or modem is ready to establish a communications link. The DSR signal is a modem status input. The CPU tests the /DSR signal by reading bit 5 (DSR) of the Modem Status Register (MSR) for the appropriate channel. Bit 5 is the complement of the DSR signal. Bit 1 (DDSR) of the MSR indicates whether the DSR input has changed state since the previous reading of the MSR. **NOTE:** *Whenever the DDSR bit of the NSR is set, an interrupt is generated if Modem Status interrupts are enabled.*
/DSTRB	76	O	EPP Data Strobe. This signal is used in EPP mode as data strobe. It is an active low signal.
/DTR1 /DTR2	69, 61	O	UARTs Data Terminal Ready. When low, this output indicates to the modem or data set that the UART is ready to establish a communications link. The DTR signal can be set to an active low by programming bit 0 (DTR) of the Modem Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.
/ERR	77	I	Parallel Port Error. This input is set low by the printer when an error is detected. This pin has a nominal 25 KOHM pull-up resistor attached to it.
/HDSEL (Normal Mode)	32	O	FDC Head Select. This output determines which side of the FDD is accessed. Active selects side 1, inactive selects side 0.
/HDSEL (PPM Mode)	77	O	FDC Head Select. This pin offers an additional Head Select signal in PPM Mode when PNF = 0.
IDLE	41	O	FDD IDLE. IDLE indicates that the FDC is in the IDLE state and can be powered down. Whenever the FDC is in IDLE state, or in power-down state, the pin is active high.
/INDEX	45	I	Index. This input signals the beginning of a FDD track.
/INDEX (Normal Mode)	92	I	Index. This pin gives an additional Index signal in PPM mode when PNF = 0.
/INIT (PPM Mode)	78	I/O	Initialize. When this signal is low, it causes the printer to be initialized. This pin is in a tristate condition 10 ns after a 1 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
IORCHDY	51	O	I/O Channel Ready. When IORCHDY is driven low, the EPP extends the host cycle.
IRQ3, 4 IRQ5-7 IRQ9-11 IRQ12, 15 (PnP Mode)	99, 98 96-94, 55-57, 66, 58	I/O	Interrupt 3, 4, 5, 6, 7, 9, 10, 11, 12, and 15. This pin can be a totem-pole output or an open-drain output. The interrupt can be sourced by one of the following: UART1 and/or UART2, parallel port, FDC, SIRQI1 pin, SIRQI2 pin or SIRQI3 pin. IRQ5 is multiplexed with ADRATE0. IRQ12 is multiplexed with /DSR2 and IRRX2. IRQ15 is multiplexed with SIRQI1.
IRQ3, 4 (Legacy Mode)	99, 98	O	Interrupt 3 and 4. These are active high interrupts associated with the serial ports. IRQ3 presents the signal if the serial channel ahs been designated as COM2 or COM4. IRQ4 presents the signal if the serial port is designated as COM1 or COM3. The interrupt is reset low (inactive) after the appropriate interrupt service routine is executed.
IRQ5 (Legacy Mode)	96	I/O	Interrupt 5. Active high output that indicates a parallel port interrupt. When enabled, this pin follows the /ACK signal input. When it is noe enabled, this signal is tri-state. This pin ia I/O only when ECP is enabled, and IRQ5 is configured.
IRQ6 (Legacy Mode)	95	O	Interrupt 6. Active high output to signal the completion of the execution phase for certain FDC commands. Also used to signal when a data transfer is ready during a non-DMA operation.
IRQ7 (Legacy Mode)	94	I/O	Interrupt 7. Active high output that indicates a parallel port interrupt. When enabled, this signal follows the /ACK signal intput. When it is not enabled, this signal is tri-state. This pin is I/O only when ECP is enabled, and IRQ7 is configured.
IRRX1 IRRX2	65, 66	I	IrDA or SHARP- Infrared Receive. One of these pins is the infrared serial data input. IRRX1 is multiplexed with SIN2. IRRX2 is multiplexed with /DSR2 and IRQ12.
IRTX	63	O	Infrared Transmit. **I**nfrared serial data output. Software configuration selects either IrDA or Sharp-IR protocol. This pin is multiplexed with SOUT2/BOUT/CFG0.
MR	100	I	Master Reset. Active high output that resets the controller to the idle state and resets all disk interface outputs to their inactive states. The DOR, DSR, CCR, Mode command, Configure command, and Lock command parameters are cleared to their default values. The Specify command parameters are not affected

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
/MSEN0 /MSEN1 (Normal Mode)	50, 49	I	Media Sense. These pins are Media Sense input pins when bit 0 of FCR is 0. Each pin has a 10 KΩ internal pull-up resistor. When bit 0 of FCR is 1, these pins are Data Rate output pins and the pull-up resistors are disabled.
/MSEN0 /MSEN1 (PPM Mode)	86, 84	I	Media Sense. These pins gives additional Media Sense signals for PPM Mode and PNF = 0.
/MTR0 /MTR1 (Normal Mode)	44, 41	O	FDC Motor Select 0, 1. These are the motor enable lines for drives 0 and 1, and are controlled by bits D7-D4 of the Digital Output register. They are active low outputs. They are encoded with information to control four FDDs when bit 4 of the Function Enable Register (FER) is set. MTR0 exchanges logical motor values with MTR1 when bit 4 of FCR is set.
/MTR1 (PMM Mode)	82	O	FDC Motor Select 1. This pin offers an additional Motor Select 1 signal in PPM mode when PNF = 0. This pin is the motor enable line for drive 1 when bit 4 of FCR is 0. It is the motor enable line for drive 0 when bit 4 of FCR 1. This signal is active low
PD	43	O	FDC Power Down. This pin is PD output when bit 4 of PMC is 1. It is /DR1 when bit 4 of PMC is 0. PD is active high whenever the FDC is in power-down state, either via bit 6 of the DSR (or bit 3 of FER, or bit 0 of PTR), or via the mode command.
PD0-7	92-89, 87-84	I/O	Parallel Port Data. These bidirectional pins transfer data to and from the peripheral data bus and the parallel port Data Register. These pins have high current drive capability.
PE	81	I	Parallel Port Paper End. This input is set high by the printer when it is out of paper. This pin has a nominal 25 KΩ pull-down resistor attached to it.
PNF	47	I	Printer Not Floppy. PNF is the Printer Not Floppy pin when bit 2 of FCR is 1. It selects the device which is connected to the PPM pins. A parallel printer is connected when PNF = 1 and a floppy disk drive is connected when PNF = 0. This pin is the DRV2 input pin when bit 2 of FCR is 0.
/RD	17	I	Read. Active low input to signal a data read by the microprocessor.
/RDATA (Normal Mode)	33	I	FDD Read Data. This input is the raw serial data read from the floppy disk drive.
/RDATA (PPM Mode)	89	I	FDD Read Data. This pin supports an additional Read Data signal in PPM Mode when PNF = 0.

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
/RI1 /RI2	68, 60	I	UARTs Ring Indicator. When low, this indicates that a telephone ring signal has been received by the modem. The /RI signal is a modem status input whose condition is tested by the CPU by reading bit 6 (RI) of the Modem Status Register (MSR) for the appropriate serial channel. Bit 6 is the complement of the RI signal. Bit 2 (TERI) of the MSR indicates whether the RI input has changed from low to high since the previous reading of the MSR. **NOTE:** *When the TERI bit of the MSR is set and Modem Status interrupts are enabled, an interrupt is generated.*
/RTS1 /RTS2	72, 64	O	UARTs Request to Send. When low, this output indicates to the modem or data set that the UART is ready to exchange data. The RTS signal can be set to an active low by programming bit 1 (RTS) of the Modem Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal to its inactive state.
SIN1 SIN2	73, 65	I	UARTs Serial Input. This input receives composite serial data from the communications link (peripheral device, modem, or data set).
SIRQ1 SIRQ2 SIRQ4	58, 49, 47	I	System interrupt 1, 2, and 3. This input can be routed to one of the following output pins: IRQ3-IRQ7, IRQ9-IRQ12. SIRQ12 and SIRQ13 can be also routed to IRQ15. Software configuration determines to which output pin the input pin is routed to. SIRQ1 is multiplexed with IRQ15, SRIQ12 is multiplexed with DRATE1/MSEN1/CS0, and SIRQ3 is multiplexed with DRV2/PNF/DR23.
SLCT	80	I	Parallel Port Select. This input is set high by the printer when it is selected. This pin has a nominal 25 KΩ pull-down resistor attached to it.
/SLIN	79	I/O	Parallel Port Select Input. When this signal is low, it selects the printer. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull this pin high using a 4.7 KΩ resistor.
SOUT1 SOUT2	71, 63	O	UARTs Serial Output. This output sends composite serial data to the communications link (peripheral device, modem, or data set). The SOUT signal is set to a marking state (logic 1) after a Master Reset operation.
/STB	93	I/O	Parallel Port Data Strobe. This output indicates to the printer that a valid data is available at the printer port. This pin is in a tristate condition 10 ns after a 0 is loaded into the corresponding Control Register bit. The system should pull high using a 4.7 KΩ.
/STEP (Normal Mode)	38	O	FDC Step. This output signal issues pulses to the disk drive at a software programmable rate to move the head during a seek operation.
/STEP (PPM Mode)	79	O	FDC Step. This pin gives an additional step signal in PPM Mode when PNF = 0.

Table 2-14 NS87336VJG Pin Descriptions (continued)

Pin	No.	I/O	Description
TC	4	I	Terminal Count. Control signal from the DMA controller to indicate the termination of a DMA transfer. TC is accepted only when FDACK is active. TC is active high in PC-AT and Model 30 modes, and active low in PS/2 mode.
/TRK0 (Normal Mode)	35	I	FDC Track 0. This input indicates the controller that the head of the selected floppy disk drive is at track zero.
/TRK0 (PPM Mode)	91	I	FDC Track 0. This pin gives an additional Track 0 signal in PPM Mode when PNF = 0.
VDDB, C	48, 97		Power Supply. This is the 3.3V/5V supply voltage for the PC87332VJG circuitry.
VSSB-E	40, 7, 88, 59		Ground. This is the ground for the PC87332VJG circuitry.
/WAIT	82	I	EPP Wait. This signal is used in EPP mode by the parallel port device to extend its access cycle. It is an active low signal.
/WDATA (Normal Mode)	37	O	FDC Write Data. This output is the write precompensated serial data that is written to the selected floppy disk drive. Precompensation is software selectable.
/WDATA (PPM Mode)	81	O	FDC Write Data. This pin provides an additional Write Data signal in PPM Mode when PNF=0. (See PE.)
/WGATE (Normal Mode)	36	O	FDC Write Gate. This output signal enables the write circuitry of the selected disk drive. WGATE has been designated to prevent glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
/WGATE (PPM Mode)	80	O	FDC Write Gate. This pin gives an additional Write Gate signal in PPM mode when PNF = 0.
/WP (Normal Mode)	34	I	FDC Write Protect. This input indicates that the disk in the selected drive is write protected.
/WP (PPM Mode)	90	I	FDC Write Protect. This pin gives an additional Write Gate signal in PPM mode when PNF = 0.
/WR	16	I	Write. An active low input to signal a write from the microprocessor to the controller.
/WRITE	93	O	EPP Write Strobe. This signal is used in EPP mode as write strobe. It is active low.
X1/OSC	5	I	Crystal1/Clock. One side of an external 24 MHz/48 MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
X2	6	O	Crystal 2. One side of an external 24 MHz/48 MHz crystal is attached here. This pin is left unconnected if an external clock is used.
/ZWS	1	O	Zero Wait State. This pin is the Zero Wait State open drain output pin when bit 6 of FCR is 0. ZWS is driven low when the EPP or ECP is written, and the access can be shortened.

2.8 Yamaha YMF715 Audio Chip

YMF715-S (OPL3-SA3) is a single audio chip that integrates OPL3 and its DAC, 16 bit Sigma-delta CODEC, MPU401 MIDI interface, joystick with timer, and a 3D enhanced controller including all the analog components which is suitable for multi-media application. This LSI is fully compliant with Plug and Play ISA 1.0a, and supports all the necessary features, i.e. 16 bit address decode, more IRQs and DMAs in compliance with PC'96. This LSI also supports the expandability, i.e. Zoomed Video, Modem and CD-ROM interface in a Plug and Play manner, and power management (power down, power save, partial power down, and suspend/resume) that is indispensable with power-conscious application.

2.8.1 Features

- Built-in OPL3
- Supports Sound Blaster Game compatibility
- Supports Windows Sound System compatibility
- Supports Plug & Play ISA 1.0a compatibility
- Full Duplex operation
- Built-in MPU401 Compatible MIDI I/O port
- Built-in Joystick
- Built-in the 3D enhanced controller including all the analog components
- Supports multi-purpose pin function (Support 16-bit address decode, DAC interface for OPL4-ML, Zoomed Video port, EEPROM interface, MODEM interface, IDE CD-ROM interface)
- Hardware and software master volume control
- Supports monaural input
- 24 mA 1TL bus drive capability
- Supports Power Management(power down, power save, partial power down, and suspend/resume) ..
- +5V/ +3.3V power supply for digital, 5V power supply for analog.
- 100 pin SQFP package (YMF715-S)

2.8.2 Pin Diagram

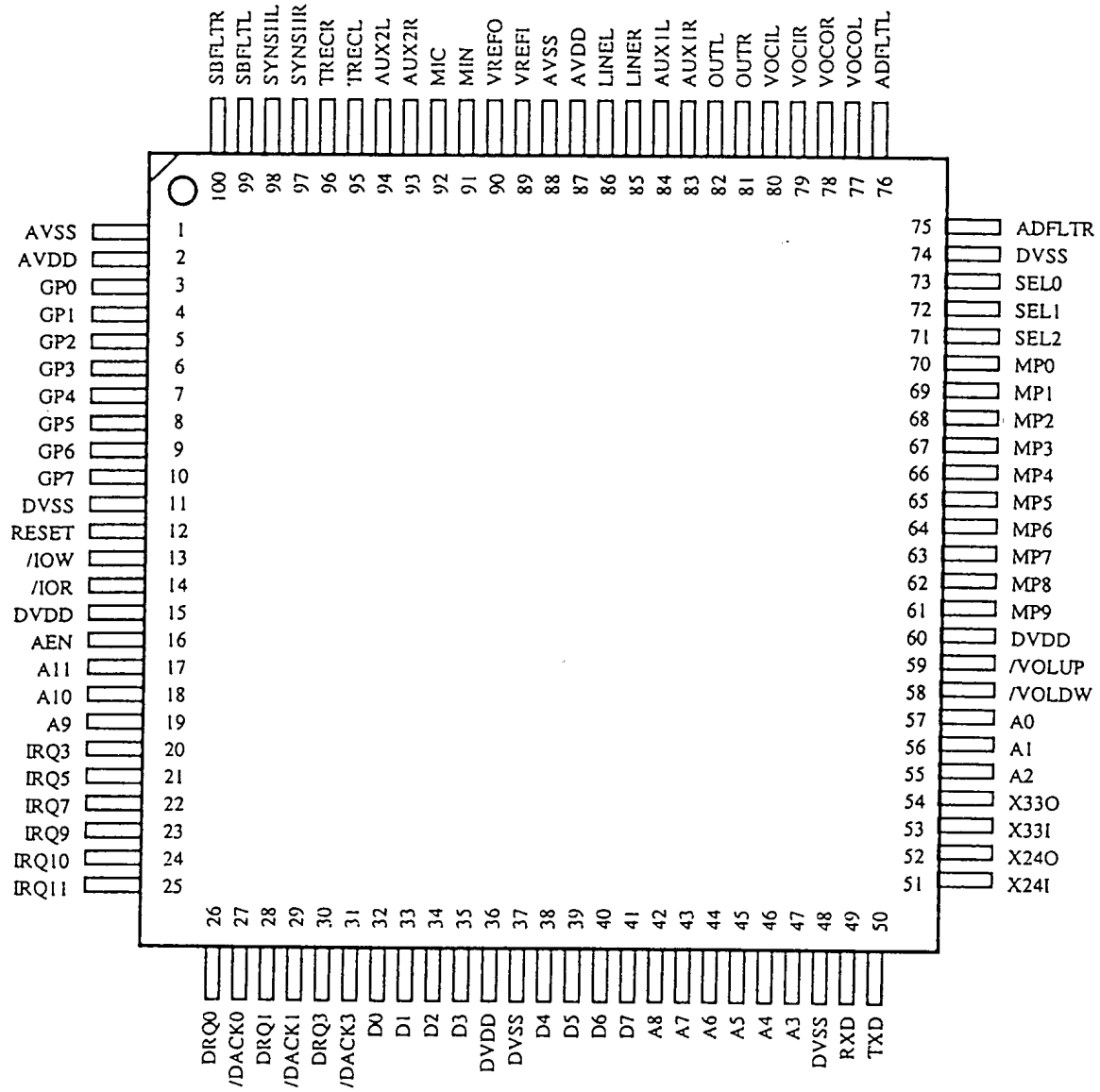


Figure 2-17 YMF715 Block Diagram

2.8.3 Pin Descriptions

Table 2-15 YMF715 Descriptions

Pin name	Pins	I/O	Type	Size	Function
ISA bus interface: 36 pins					
D7-0	8	I/O	TTL	24mA	Data Bus
AI 1-0	12	I	TTL	2mA	Address Bus
AEN	1	I	TTL	2mA	Address Bus Enable
/IOW	1	I	Schmitt	4mA	Write Enable
/IOR	1	I	Schmitt	4mA	Read Enable
RESET	1	I	Schmitt	4mA	Reset
IRQ3,5,7,9,10,11	6	T	TTL	12mA	Interrupt request
DRQ0,1,3	3	T	TTL	12mA	DMA Request
/DACK0, 1,3	3	I	TTL	2mA	DMA Acknowledge
Analog Input & Output : 24 sins					
OUTL	1	O	-	-	Left mixed analog output
OUTR	1	O	-	-	Right mixed analog output
VREFI	1	I	-	-	Voltage reference input
VREFO	1	O	-	-	Voltage reference output
AUXIL	I	I	-	-	Left AUX1 input
AUX1R	I	I	-	-	Right AUX1 input
AIJX2L	I	I	-	-	Left AUX2 input
AUX2R	1	I	-	-	Right AUX2 input
LINEL	1	I	-	-	Left LINE input
LINER	1	I	-	-	Right LINE input
MIC	1	I	-	-	MIC input
MIN	1	I	-	-	Monaural input
TRECL	1	-	-	-	Left Treble capacitor
TRECR	1	-	-	-	Right Treble-capacitor
SBFLTL	1	-	-	-	Left SBDAC filter
SBFLTR	1	-	-	-	Right SBDAC filter
SYNSHL	1	-	-	-	Left SYNDAC sample / hold capacitor
SYNSHR	1	-	-	-	Right SYNDAC sample / hold capacitor
ADFLTL	1	-	-	-	Left input filter
ADFLTR	1	-	-	-	Right input filter
VOCOL	1	O	-	-	Left voice output
VOCOR	I	O	-	-	Right voice output
VOCIL	1	I	-	-	Left voice input
VOCIR	1	I	-	-	Right voice input

Table 2-15 YMF715 Descriptions (Continued)

Pin name	Pins	I/O	Type	Size	Function
Multi-purpose Dins: 13 pins					
SEL2-0	3	I+	CMOS	2mA	Refer to “Multi-purpose pins” section
MP9-0	I0	I+/O	TTL	4mA	Refer to “multi-purpose pins” section
Others: 27 pins					
GPO - GP3	4	IA	-	-	Game Port
GP4- GP7	4	I+	Schmitt	2mA	Game Port
RXD	1	I+	Schmitt	2rnA	MIDI Data Receive
TXD	1	O	TTL	4mA	MIDI Data Transfer
/VOLUP	1	I+	Schmitt	2mA	Hardware Volume (Up)
/VOLDW	I	I+	Schmitt	2mA	Hardware Volume (Down)
X331	1	I	CMOS	2mA	33.8688 MHz
X33O	1	O	CMOS	2mA	33.8688 MHz
X24I	1	I	CMOS	2mA	24.576 MHz
X24O	1	O	CMOS	2mA	24.576 MHz
AVDD	2	-	-	-	Analog Power Supply (put on +5.0V)
DVDD	3	-	-	-	Digital Power Supply (put on +5.0 V or +3.3V)
AVSS	2	-	-	-	Analog GND
DVSS	4	-	-	-	Digital GND

Note: I+: Input Pin with Pull up Resistor
Schmitt: TTL-Schmitt input pin
T: TTL-tri-state output pin
O+: Output Pin with Pull up Resistor

2.9 T62.062.C Battery Charger

2.9.1 Overview

Ambit T62.062.C.00 charger is designed exclusively for TI Extensa 610 notebook computer as a power management and battery charger module which can charge a 9 cells Nickel-Metal Hydride (NiMH) or 9 cells with 3's parallel and 3's serial Lithium Ion(LIB) Battery pack. When charging the NiMH battery , the determination of the battery full capacity for the charger is based on zero delta Voltage (0 V), temperature increment gradient (T/t), minus delta voltage (-V) and maximum voltage (Max. V). On the other hand, if charging the LIB battery, constant current and constant voltage the typical LIB battery charging mode will be applied precisely. It is important to notice that every battery pack to be used must have a built-in 103AT-2 NTC thermistor (maximum 70thermal breaker included for NiMH battery). Otherwise, most of the charger functions so as to be failed.

The charger permits a soft charging of NiMH battery to full capacity whereas over-charging is well protected. Fast charge begins with the application of the external AC adapter or the replacement of a new plugged in battery whichever NiMH or LIB battery. For safety, at the beginning of charging, battery will not be charged until its temperature within a certain interval and if start voltage is lower than another certain value, the charger module provides trickle charge current to charge the battery which prevents fast charging could possibly damage the battery. In addition, maximum temperature protection and safe timer is provided during quick charge. To maintain the capacity once the NiMH reaches full energy level, trickle charge current will be continuously provided to the battery by the charger.

2.9.2 Features

- Designed for charging a 9 cells Nickle-Metal Hydride Battery pack or 9 cells (3 parallel, 3 serial) Lithium- Ion Battery pack
- Providing the basic power management for the main system
- System off time selectable : 50mS (software) / 2.5S (hardware)
- Providing charging function whenever system in use power or not
- Providing battery protections by constantly monitoring temperature, voltage and charging time
- Compact size & low cost
- Determination of a NiMH battery full capacity against over-charging based on
  - 0 ΔV (disabled when system sharing the power with the charger during charging)
  - - ΔV (disabled when system sharing the power with the charger during charging)
  - $\Delta T/\Delta t$ (3^{o}c/3min)
  - Max. V (charge NiMH:16.2v)
- Charging LIB battery following the constant current then constant voltage mode
- Providing battery safety protections by:
  - Trickle current when battery voltage being very low

- Max. T
- Safety charging timer
- Battery temperature constantly monitoring
- Over voltage protect 13V

- Providing low battery warning signals when the system using battery as the main power source

2.9.3 Absolute Maximum Ratings

Table 2-16 T62.062.C Absolute Maximum Ratings Table

Parameter	Maximum Ratings
Supply voltage (Adapter)	0V to +24V
Output current	3A
Total sink current of all O/P pin (output pin to DC/DC not included)	15mA
Charge current	1.9A
Operating temperature	0 to 60
Storage temperature	-10 to 85

2.9.4 Electrical Characteristics

Table 2-17 T62.062.C Electrical Characteristics Table

Parameter	Symbol	Condition	MIN	TYP	MAX	UNITS
INPUT						
External Adapter	AC power	*Note 1	19	20	21	V
Disable (High)	Disable	Delay about 10 ms	3.5	5	5.25	V
(Low)			-	-	0.7	V
(Supply current)			300	-	-	uA
System in use power (High)	S.I.U.		4.0	5	5.25	V
(Low)			-	-	2.0	V
(Supply current)			1	-	-	mA

Table 2-17 T62.062.C Electrical Characteristics Table (Continued)

Parameter	Symbol	Condition	MIN	TYP	MAX	UNITS
OUTPUT						
AC Source input Signal (Voltage) (Supply current)	AD5V	AC source voltage > 8V	4.5	5	5.25 10	V mA
Battery in use (High) (Low) (Supply current)	BAT-IN-USE#	@I load=100uA	2.7	5	5.25 0.7 100	V V uA
Power Output	DCBAT OUT		-	-	3	A
Charge Indicator (High) (Low) (Supply current)	BT-QCHG	Quick	 3.5 - -	 5 - -	 5.25 0.8 100	 V V uA
Battery Low 1 (High) (Low) (Supply Current)	BL1#	@I load=100uA	 2.7 - -	 5 - -	 5.25 0.7 100	 V V uA
Battery Low 2 (High) (Low) (Supply Current)	BL2#	@I load=100uA	 2.7 - -	 5 - -	 5.25 0.7 100	 V V uA
BATTERY LOW VOLTAGE WARNING SIGNAL						
Battery Low 1 (NiMH) (LIB)		@25 TC125PPM/	10.53 8.50	10.70 8.65	10.86 8.80	V
Battery Low 2 (NiMH) (LIB)		@25 TC125PPM/	10.19 8.08	10.35 8.23	10.50 8.38	V
Battery Low 3 (NiMH) (LIB)		@25 TC125PPM/	9.07 7.58	9.22 7.73	9.36 7.88	V
CHARGE PARAMETER						
External Adapter Charge current		System not in use System in use	1.8 0.58	1.9 0.65	2.0 0.72	A A
DC OPERATION (@25 Vin=10.8V)						
Total Module Current Consumption (output pin not included)		**System on** **System off**		**2.3** **150**		**mA** **uA**

Table 2-17 T62.062.C Electrical Characteristics Table (Continued)

Parameter	Symbol	Condition	MIN	TYP	MAX	UNITS
SAFETY OPERATION						
Over voltage protect by Software		NiMH LiB_Ion		16.2 13		V V
Note 1: External Adapter: Voltage limit 20V1V with maximum 24V over voltage as well as over current protection.						

2.9.5 Pin Diagram

DC_BAT_OUT	1 o	o 2	DC_BAT_OUT
DC_BAT_OUT	3 o	o 4	DC_BAT_OUT
GND	5 o	o 6	GND
PERIPHERAL SYSTEM ON	7 o	o 8	5VSB_OUT
SYSTEM ON	9 o	o 10	DISABLE
BT_QCHG	11 o	o 12	AD5V
SMI	13 o	o 14	S.I.U.
TH	15 o	o 16	BL1#
ID	17 o	o18	BL2#
GND	19 o	o20	BAT_IN_USE#
BT_VS	21 o	o22	GND
BT+	23 o	o24	BT+
BT+	25 o	o26	BT+

Figure 2-18 T62.062.C Pin Diagram

2.9.6 Pin Description

Table 2-18 T62.062.C Pin Description table

Item	Pin Name	I/O	Description
SAFETY OPERATION			
1	DC_BAT_OUT	O/P	.adapter power input and battery power output terminal(with 5 A short circuit protection)
2	DC_BAT_OUT	O/P	same as pin 1
3	DC_BAT_OUT	O/P	same as pin 1
4	DC_BAT_OUT	O/P	same as pin 1
5	GND		ground
6	GND		ground
7	PERIPHERAL SYSTEM ON	I/P	system power on ,input a high pulse. user have different way to turn on sysem by peripheral device.
8	5VSB_OUT	O/P	charger 5VSB output
9	SYSTEM ON	O/P	connecting to main system ‘power on ’ signal
10	DISABLE	I/P	logic high to notice charger to turn off system
11	BT-QCHG	O/P	charge status, when quick charge output logic high.
12	AD5V	O/P	when adapter inserted, output +5V,10mA (max).
13	SMI	O/P	open collector, when push power on switch then output low. (delay 6040 mS)
14	S.I.U.	I/P	logic high when system in use power
15	TH	I/P	connecting to thermistor inside battery pack using 103AT-2 (10K/25,1%).
16	BL1#	O/P	when battery voltage lower than BL1 voltage then output low (available when S.I.U).
17	ID	I/P	open circuit when a 9 cells LIB battery inserted, connecting to GND when a 9 cells NiMH battery inserted.
18	BL2#	O/P	when battery voltage lower than BL2 voltage then output low (available when S.I.U).
19	GND.		.
20	BAT-IN-USE#	O/P	logic low when battery in use power (available when S.I.U).
21	BT_VS	I/P	connecting to battery most positive terminal
22	GND		
23	BT+	I/O	connecting to battery most positive terminal
24	BT+	I/O	same as pin 23
25	BT+	I/O	same as pin 23
26	BT+	I/O	same as pin 23

2.9.7 Functions Description

2.9.7.1 Charge Function

A. FOR NIMH BATTERY

When the charger module charges a 9 cells NiMH battery, 0V and T/ t, max T and - v detentions will be used as the main methods to determine the full charged battery. To ensure safety for the battery and system, fast charging NiMH battery after long period of storage time, the module will disable 0V detection during a short " hold-off" period at the start of fast charging. Also when 'charge in use' the 0V and -V detection will be disabled during whole charging period.

When system not in use power, the quick charge current will be limited by the Adapter to 1.9A0.1A. If system in use the charge current will be limited by charger module to 0.650.07A. When battery voltage lower than 1.0v/cell the charger module will precharge the battery (with 1/8 duty cycle/2HZ) and 50/150 minutes maximum timer.

When battery is fully charged, the charger module will offer 25mA 5mA trickle current to maintain the battery at 100% capacity.

The BT-QCHG pin will send a logic high signal for LED indication by the charger, when precharge or quick charge is on.

B. FOR LIB BATTERY

When the charger module charges a 9 cells (3's parallel , 3's serial) LIB battery. The charger will offer 1.90.1A charger current when system not in use power whereas 0.650.07A when system in use power. Quick charge will be terminated when charge current less then 150mA60mA. Then 12.67V 0.05V constant voltage with one hour timer will be applied to charge battery. Also if battery voltage lower than 7.50.2V the charger will precharge the battery, using 200mA60mA with 2 hours maximum timer.

When battery is fully charged the charger module stop charge. But the charger module will recharge the battery if battery voltage lower then 11.4V 0.2V.

The BT-QCHG pin will send a logic high signal for LED indication, when precharge or quick charge is on.

2.9.7.2 Discharge Function

When system turned on, the charger will check AC power inserted or not . If AC power inserted, then AC power will be the role of power provider. If not, the charger will discharge the battery already inserted in the notebook system.

If system in use power when Adapter not inserted and battery voltage lower than BL1 voltage, the charger module will indicate a battery Low 1 signal . And if battery voltage lower than BL2 voltage , the charge will indicate a Battery Low 2 signal .

When system on if Adapter not inserted and battery voltage lower than BL3 voltage , then system will be turned off by the charger module.

In addition, when system sends a ‘disable’ signal to charger module, system will be turned off by the charger module immedietly.

2.9.7.3 Safety Concerns

For safety, the charger module inhibits charging until the battery voltage and temperature are within the configured ranges. If the voltage is less than the low voltage threshold , the charger module provides trickle current to charge the battery . This prevents fast charging could possibly damage the battery. Also when the temperature of battery pack is over the temperature threshold, the charger module will not charge the battery until its temperature within a configured range. This prevents reducing the battery’s service life.

Concludely, in order to ensure safety for the battery and system, charge may be terminated when the battery temperature over a threshold or after a safety time period.

2.10 T62.061.C DC-DC Converter

This compact, high efficiency DC/DC Converter features +5V, +3.3V, 2.35V/2.45V/2.9V/3.1V, +12V and +6V five outputs up to 22 watts. And it accepts input from 7V to 21V, suitable for 3 cells Lithium Ion or 10 cells NiMH battery input Pentium based Notebook PC.

The converter also supplies P.G. signal, 2.35V/2.45V/2.9V/3.1V switch for CPU and ON/OFF control.

2.10.1 Pin Diagram

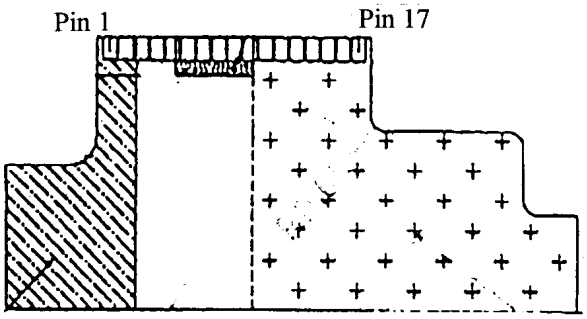


Figure 2-19 T62.061.C Pin Diagram

2.10.2 Pin Assignment

Table 2-19 T62.061.C Pin Descriptions

Pin No.	Description
1,2	GND
3	DC-IN
4	P.G.Vcc
5	+5.0V
6	GND
7	+6V
8	+12V
9	GND
10	+3.3V
11	5VSB
12	ON/OFF
13	P.G.
14,15	Vcpu
16,17	GND

2.10.3 Specifications

Input:

- DC BATT_IN:7V-8V DC

Output:

- **+**5V :Load :0~2A
- +12V :Load :0~0.12A
- The other conditions same as 2.2.1

Input:

- DCBATT_IN :8V-21V DC

Output:

- +5V: Load : 0A-3.2A Regulation: +5%, -5%
  - Ripple: 50mV (max)
  - Noise: 100mV (max)
  - OVP: 6.5-8.2V
  - Short-circuit protection
  - Fuse protection
  - *Ripple(max)=75mV when regulate in IDLE mode
- +3.3V: Load : 0A-3.3A Regulation: +5%, -5%
  - Ripple: 50mV (max)
  - Noise: 100mV (max)
  - OVP: 4.5-6.2V
  - Short-circuit protection
  - Fuse protection
  - *Ripple(max)=75mV when regulate in IDLE mode
- +2.9V:(3.1V) Load : 0A-3.0A Regulation: +5%, -4%
  - Ripple: 50mA (max)
  - Noise: 100mV (max)
  - OVP: 3.3-5.0V
  - Short-circuit protection
  - Fuse protection
  - *Ripple(max)=75mV when regulate in IDLE mode

- +2.35V:(2.45V) Load : 0A-4.2A Regulation: +5%, -4%
  - Ripple: 50mA (max)
  - Noise: 100mV (max)
  - OVP: 3.3-5.0V
  - Short-circuit protection
  - Fuse protection
  - *Ripple(max)=75mV when regulate in IDLE mode
- +12V : Load : 0A-0.15A Regulation: +/-5%
  - Ripple: 100mV (max)
  - Noise: 200mV (max)
  - OVP: 14-20V
  - *The +12V max load condition is available only when the +5V output load is greater than 0.5A.
- +6V : Load : 0A~0.1A Regulation: 5.5V~7.5V
  - Ripple: 300mV (max)
  - Noise: 500mV (max)
  - OVP: 7-9 V
  - *The +6V max load condition is available only when the +5V output load is greater than 0.5A.
- 5VSB:Load : 5mA Regulation:+/-10%
  - Ripple: 75mV(max) Noise: 250mV(max)
  - P.G. :Active high within 100ms to 500ms after system s +5V, 3.3V and Vcpu are all in regulation.
  - Driving capability:12uA(source) 200uA(sink)

2.10.4 Control

- VCPU Control: Control switch can switch Vcpu output voltage to 2.35V2.45V2.9 or 3.1V.
- ON/OFF: A logic low will turn off +5V,+3.3V, 2.35V/2.45V/2.9V/3.1V,+12V and +6V main o/p. The DC/DC converter draws about 30uA when the notebook computer is in shutdown mode.

2.10.5 Application:

Input filter capacitor

The recommended value is two pieces of 10uf/50V ceramic capacitor(or the same grade capacitor, such as SANYO OS-CON capacitor) with less than 150mohm ESR. And it should be located less than 10mm away from DCBATT_IN pin.

Output filter capacitor

The recommended value is 30uF/Amps TAN or OS-CON CAP.

Efficiency:

90%(MIN) at 12V input and 5V/1.5A , 3.3V/0.8A , 2.9V/0.6A load.

Environment:

- Operating
  - Temperature: 0 to 65
  - Relative Humidity: 10% to 95%
- Shipping/Storage
  - Temperature: 25 to 85
  - Relative Humidity: 10% to 95%

2.11 T62.064.C DC-AC Inverter (11.3")

THIS IS A DC-AC INVERTER UNIT TO DRIVE BACKLIGHT CCFT FOR NOTEBOOK COMPUTERS

Table 2-20 MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
INPUT VOLTAGE	Vin	7	22	V	
INPUT CURRENT	Iin	--	0.6	A	

2.11.1 Electrical Specifications

Electrical Characteristics

Table 2-21 Electrical Characteristics

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
INPUT VOLTAGE	Vin	7.0	--	22.0	V	
INPUT CURRENT	Iin	--	--	600	mA	
NO LOAD VOLATAGE	Vs	--	--	1400	Vrms	
WORKING FREQUENCY	f	45	--	60	KHz	
TUBE CURRENT (OUTPUT MAX.)	Iout	5.5	6.0	6.5	mArms	PWM 100%
TUBE CURRENT (OUTPUT MIN.)	Iout	0.5	1.0	1.5	mArms	PWM 25%
CONTRAST VOLTAGE (OUTPUT MAX)	VEE	2.15	2.3	2.45	Vrms	PWM 100%
CONTRAST VOLTAGE (OUTPUT MIN)	VEE	1.35	1.5	1.65	mArms	PWM 25%
Tc=25 Vin=7.0V TO 22.0V						

Operation Conditions

- OPERATING TEMPERATURE 0 TO +50
- OPERATING HUMIDITY 90% MAX. R.H
- STORAGE TEMPERATURE 10 TO +85
- STORAGE HUMIDITY 90% MAX. R.H
- MTBF 50000 HRS

2.11.2 Pin & Connector Assignment

J1: 52103-1217 (MOLEX)

Table 2-22 Pin Description

PIN NO.	SYMBOL	DESCRIPRION
1	DCBATTIN	DC (7.0V ~ 21.0V)
2	GND	POWER GND
3	CCFTON	PWM SIGNAL FOR ON/OFF AND BRIGHTNESS CONTROL
4	DATA	ID X24C02 DATA
5	+5.0V	+5.0V ± 10%
6	SGND	LOGIC GND FOR X24C02
7	N.C.	
8	CK	CLOCK FOR X24C02
9	N.C.	
10	VEE	VEE OUTPUT
11	CTEN	CONTRAST ON/OFF TTL LEVEL ″H″ ON
12	CTVREN	PWM SIGNAL FOR CONTRAST VOLTAGE

J2:SM02(8.0)B-BHS-1-TB2P (JST)

Table 2-23 Pin Description

PIN NO.	SYMBOL	DESCRIPRION
1	VOUT1	Lanp , Input HV
2	NC	
3	VOUT2	Lanp , Input LV

2.11.3 Top Overlay

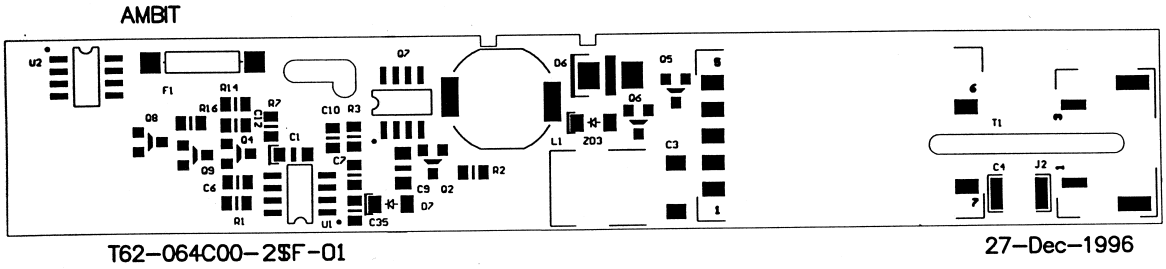


Figure 2-20 T62.064.C DC-AC Inverter Top Overlay diagram

2.11.4 Bottom Overlay

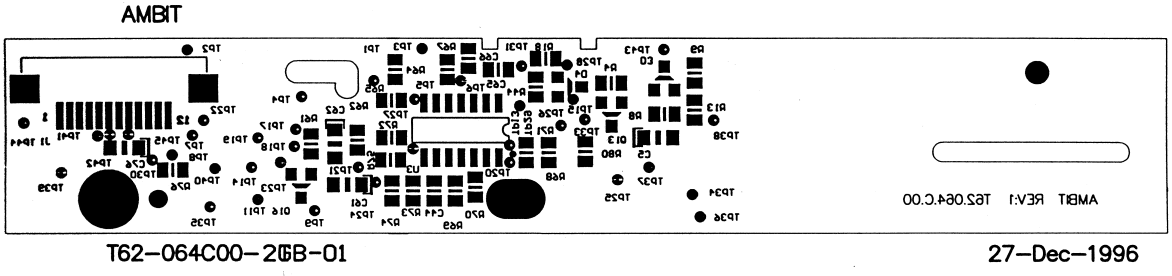


Figure 2-21 T62.064.C DC-AC Inverter Bottom Overlay diagram

2.12 T62.066.C DC-AC Inverter (12.1")

This is a DC-AC inverter unit to drive Backlight CCFT for notebook computers

Table 2-23 MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
INPUT VOLTAGE	Vin	7	21	V	
INPUT CURRENT	Iin	--	0.65	A	

2.12.1 Electrical Specifications

Electrical Characteristics

Table 2-24 Electrical Characteristics

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
INPUT VOLTAGE	Vin	7.0	--	21.0	V	
INPUT CURRENT	Iin	--	--	650	mA	
NO LOAD VOLATAGE	Vs	--	--	1400	Vrms	
WORKING FREQUENCY	f	45	--	60	KHz	
TUBE CURRENT (OUTPUT MAX.)	Iout	5.5	6.0	6.5	mArms	PWM 100%
TUBE CURRENT (OUTPUT MIN.)	Iout	0.5	1.0	1.5	mArms	PWM 25%
Tc=25 Vin=7.0V TO 21.0V						

Operation Conditions

- OPERATING TEMPERATURE 0 TO +50
- OPERATING HUMIDITY 90% MAX. R.H
- STORAGE TEMPERATURE 10 TO +85
- STORAGE HUMIDITY 90% MAX. R.H
- MTBF 50000 HRS

2.12.2 Pin & Connector Assignment

J1: 52103-1217 (MOLEX)

Table 2-25 J1: 52103-1217 (MOLEX) Pin Description

PIN NO.	SYMBOL	DESCRIPRION
1	DCBATTIN	DC (7.0V ~ 21.0V)
2	GND	POWER GND
3	CCFTON	PWM SIGNAL FOR ON/OFF AND BRIGHTNESS CONTROL
4	DATA	ID X24C02 DATA
5	+5.0V	+5.0V ± 10%
6	SGND	LOGIC GND FOR X24C02
7	N.C.	
8	CK	CLOCK FOR X24C02
9	N.C.	
10	VEE	VEE OUTPUT
11	CTEN	CONTRAST ON/OFF TTL LEVEL ″H″ ON
12	CTVREN	PWM SIGNAL FOR CONTRAST VOLTAGE

J2:SM02(8.0)B-BHS-1-TB2P (JST)

Table 2-26 J2:SM02(8.0)B-BHS-1-TB2P (JST) Pin Description

PIN NO.	SYMBOL	DESCRIPRION
1	VOUT1	Lanp , Input HV
2	NC	
3	VOUT2	Lanp , Input LV

2.12.3 Top Overlay

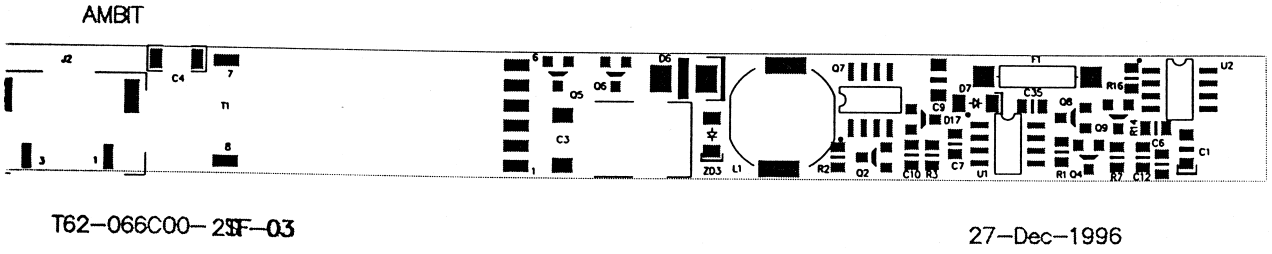


Figure 2-22 T62.066.C DC-AC Inverter Top Overlay diagram

2.12.4 Bottom Overlay

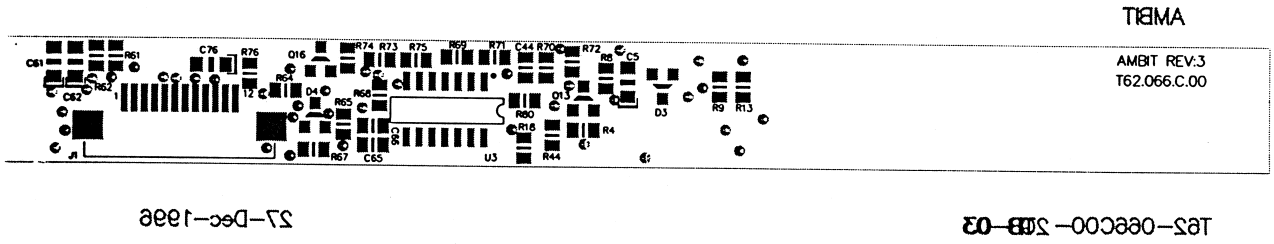


Figure 2-23 T62.066.C DC-AC Inverter Bottom Overlay diagram

BIOS Setup Information

The notebook has a BIOS setup utility that allows you to configure the notebook and its hardware settings. This chapter tells how to use the Setup utility and describes each parameter item in the setup screens.

The notebook is also bundled with Windows 95-based notebook management utility similar in function with the BIOS Setup utility called the Notebook manager. See section 5.3 for details.

3.1 When to Use Setup

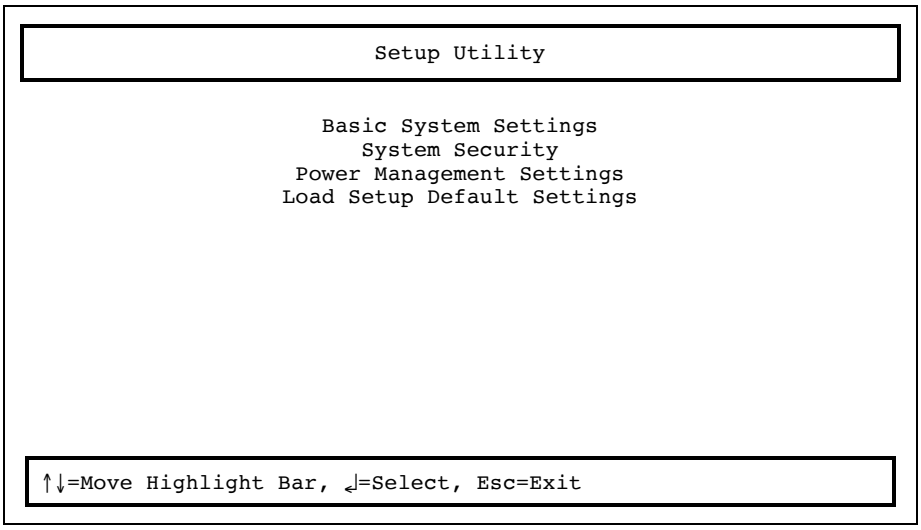
The notebook is already correctly configured for you and you do not need to run Setup. If you make any changes to the notebook or you receive an Equipment Configuration Error message after you turn on the notebook, you need to run Setup. Run Setup also if you want to do any of the following:

- Change the system date, time or speed
- Add or remove serial and parallel devices
- Change the system boot drive or display device
- Set the video display features
- Set the power-saving modes
- Set, change, or remove a system password

The system configuration values reside in the battery-powered CMOS RAM.

3.2 Entering Setup

Press F2 during POST to enter Setup. The BIOS Utility main screen displays.



There are four main menu items:

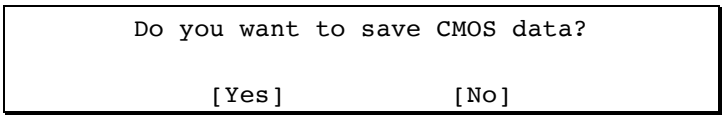
- Basic System Settings
- System Security
- Power Management Settings
- Load Setup Default Settings

Read through the Setup Screen Notes before navigating the Setup screens.

SETUP SCREEN NOTES

- From the main menu, press ↑, ↓, ← or → to move from one menu item to another and press **Enter** to enter the selected menu.
- When accessing multi-page sections, press **PgDn** and **PgUp** to go through the pages.
- Parameters displayed in low brightness (grayed-out) are not user-configurable. The notebook detects and sets the values for these parameters.
- Press ↑ or ↓ to move from one parameter to another. Press ← or → to change parameter settings. You have to change some settings when you add a component to the notebook.
- Most of the Setup parameters are self-explanatory. Press **F1** for help on individual parameters.

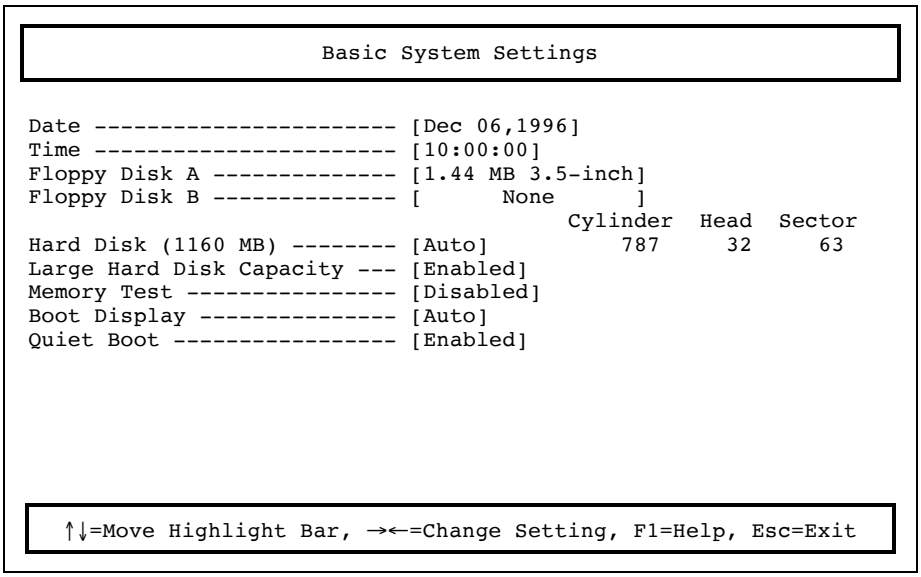
- When you press **Esc** to exit the Setup utility, the following prompt appears:



- Select `[Yes]` to save the changes you made to the configuration values or `[No]` to abandon the changes and retain the current values.

3.3 Basic System Configuration

Basic System Configuration has a one-page screen display illustrated below.



3.3.1 Date and Time

The notebook displays the current date in MM/DD/YY format and the current time in HH:MM:SS format. It uses a 24-hour clock; for example, 6:25 PM displays as 18:25:00.

3.3.2 Floppy Disk Drives

The default setting for Diskette Drive A is `[1.44 MB 3.5-inch]` and this setting applies to both an internal and external floppy drive configuration. Diskette Drive B, by default, is set to `[None]`. Enable this parameter if two floppy drives are connected to the notebook.

3.3.3 Hard Disk Drive

The default setting for IDE Drive 0 is `[Auto]`. With this setting, the BIOS automatically detects your drive parameters. You can also opt to key in your drive parameters by setting this parameter to `[User]`. To determine your drive parameters, look at the data on the label pasted on your hard disk drive (or supplied in vendor documentation) and type in the parameters. Be sure to set the correct drive parameters; otherwise an error message appears when you boot up the notebook. We suggest you set this parameter to `[Auto]`.

3.3.4 Large Hard Disk Capacity

The default setting for Large Hard Disk Capacity is `[Enabled]`. Set this parameter to `[Disabled]` if you use the UNIX operating system on this computer.

3.3.5 Memory Test

The notebook can test main memory for errors when you turn it on. The default setting, `[Disabled]`, allows the notebook to bypass the memory test and speed up the self-test procedure.

3.3.6 Boot Display

If you connect an external monitor, you can switch display between the LCD and the external display. This parameter determines which display device the notebook uses on boot-up. Table 3-1 describes the different settings.

If notebook resolution is set at 640x480, the image on the notebook and external monitor will not be full-screen. For full-screen image, set-up notebook at 800x600 resolution.

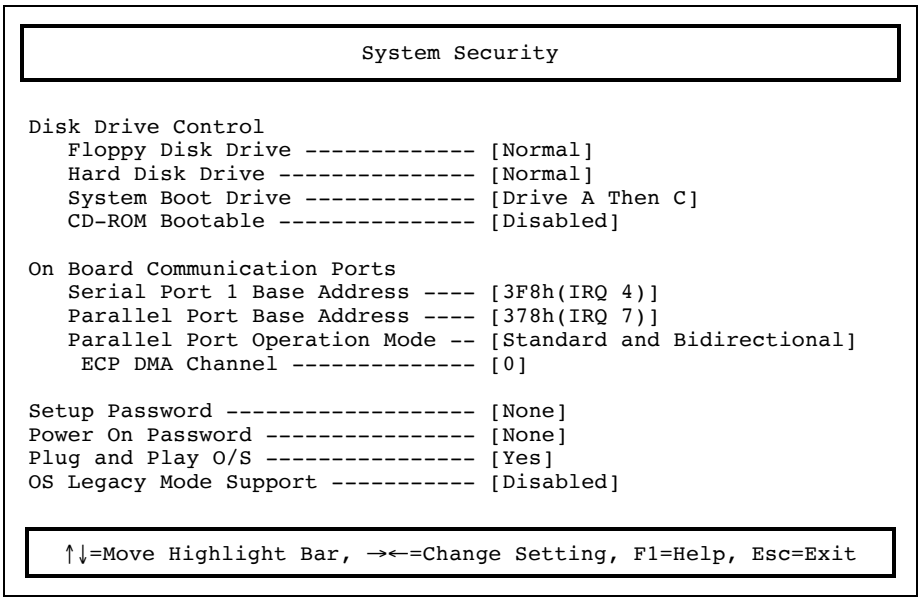
Table 3-1 Display Device Settings

Setting	Description
Auto (default)	If an external display is present, the notebook uses the external display; otherwise, the LCD is the display device.
Both	The notebook uses the external display and LCD simultaneously.

3.3.7 Quiet Boot

In Quiet Boot mode, the notebook does not display POST messages on your display. The default setting is `[Enabled]`.

3.4 System Security



3.4.1 Floppy Disk Drive Control

This parameter allows you to enable or disable the read/write functions of the floppy drive. The following table summarizes the available options.

Table 3-2 Floppy Disk Drive Control Settings

Setting	Description
Normal (default)	Floppy drive functions normally
Write Protect Boot Sector	Disables the floppy drive write function on a diskette's boot sector. This option is for operating systems that access the floppy drive 100 percent via BIOS only.
Disabled	Disables the floppy drive

3.4.2 Hard Disk Drive Control

This parameter allows you to enable or disable the read/write functions of the hard disk drive. The following table summarizes the available options.

Table 3-3 Hard Disk Drive Control Settings

Setting	Description
Normal (default)	Hard disk drive functions normally
Write Protect Boot Sector	Disables the hard disk drive write function on the hard disk's boot sector. This option is for operating systems that access the hard disk 100 percent via BIOS only.
Disabled	Disables the hard disk drive

3.4.3 System Boot Drive Control

This parameter determines which drive the notebook boots from when you turn it on. The following table lists the three possible settings.

Table 3-4 System Boot Drive Control Settings

Setting	Description
Drive A Then C (default)	Notebook boots from floppy drive A. If there is no system disk in drive A, the notebook boots from hard disk C. If the hard disk is a non-system disk, an error message appears.
Drive C Then A	Notebook boots from hard disk C. If hard disk C is not a system disk, the notebook boots from floppy drive A. If no diskette is present or if the diskette in floppy drive A is a non-system disk, an error message appears.
Drive C	Notebook boots from hard disk C. If hard disk C is not a system disk, an error message appears.
Drive A	Notebook boots from floppy drive A. If no diskette is present or if the diskette in floppy drive A is a non-system disk, an error message appears.

An installed PCMCIA bootable card overrides the System Boot Drive setting. The notebook supports SRAM card boot.

3.4.4 CD-ROM Bootable

When enabled the notebook checks the CD-ROM drive first and boots from there, if possible, before checking the System Boot Drive control setting.

There are two image types/formats for CD-ROMs - floppy drive and hard disk. See Table 3-5 for a description.

Table 3-5 CD-ROM Image Descriptions

Image Type	Upon Boot-up…
Floppy Drive	CD-ROM drive becomes drive A and the floppy drive becomes drive B. The hard disk drive remains drive C.
Hard Disk	CD-ROM drive becomes drive C and the hard disk drive becomes drive D. The floppy drive remains drive A.

3.4.5 Serial Port 1 Base Address

The serial port can accommodate a modem, serial mouse, serial printer, or other serial devices. The default setting for the serial port base address is `3F8h(IRQ 4)`[1].

Other options include:

- `2F8h(IRQ 3)`
- `3E8h(IRQ 4)`
- `2E8h(IRQ 3)`
- `Disabled`

Make sure the serial port base address does not conflict with the address used by a PCMCIA card, if one is installed.

3.4.6 Parallel Port Base Address

The parallel port can accommodate a parallel printer or other parallel devices. The default setting for the parallel port base address is `[378h(IRQ 7)]`[1]. The other options for this parameter are:

- `278h(IRQ 5)`
- `3BCh(IRQ 7)`
- `Disabled`

3.4.7 Parallel Port Operation Mode

The parallel port supports four operation modes:

- `Standard and Bidirectional`
- `Extended Capabilities Port(ECP)`
- `Standard and Unidirectional`
- `Enhanced Parallel Port(EPP)`

ECP or Extended Capabilities Port supports a 16-byte FIFO (first in, first out) which can be accessed by host DMA cycles and PIO cycles. ECP boosts I/O bandwidth to meet the demands of high-performance peripherals. EPP or Enhanced Parallel Port is a parallel port interface that greatly improves performance for bi-directional block-mode data transfers. EPP provides greater throughput by supporting faster transfer times and a mechanism that allows the host to address peripheral device registers directly.

1 The parameter value is the base address expressed in hexadecimal.

The default setting is [Standard and Bidirectional].

If you set EPP as the parallel port operation mode, do not use 3BCh as the parallel port base address; otherwise, I/O conflicts may occur.

ECP DMA Channel

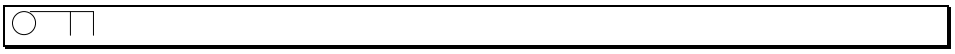
Set the ECP DMA Channel parameter if you set the Parallel Port Operation Mode to [Enhanced Capabilities Port(ECP)]. The default value, with ECP selected, is [0].

3.4.8 Passwords

Two passwords are implemented in this notebook. The Setup Password prevents unauthorized access to the Setup utility, while the Power On Password prevents unauthorized access to the notebook during boot-up and resume from hibernation.

Setting a Password

To set a password, select the desired password (Setup and Power On) to set or edit, and press ← or →. The password prompt (a key) appears:



A message below the menu prompts you to enter a password. The password may consist of up to seven characters which do not appear on the screen when you type them. After typing your password, press Enter. Another prompt appears asking you to retype your password to verify your first entry.

After setting a password, the notebook sets this parameter to [Enabled]. The next time you boot the notebook, resume from hibernation mode or run the Setup utility, the password prompt appears. Key in the appropriate password (Power On or Setup). If the password you entered is incorrect, an "X" appears. You have three chances to type in the correct password. After three tries, the following message appears:

```
Incorrect password specified.  System disabled.
```

The notebook freezes up and disables all devices. You must turn off the notebook and turn it on again to retry. If you forget your password, you must reset the configuration values stored in CMOS to defaults. Resetting CMOS requires opening up the notebook, so contact your dealer for assistance.

Removing a Password

To remove a password, select the desired password (Setup and Power On) to remove and press ← or → to set it to [None].

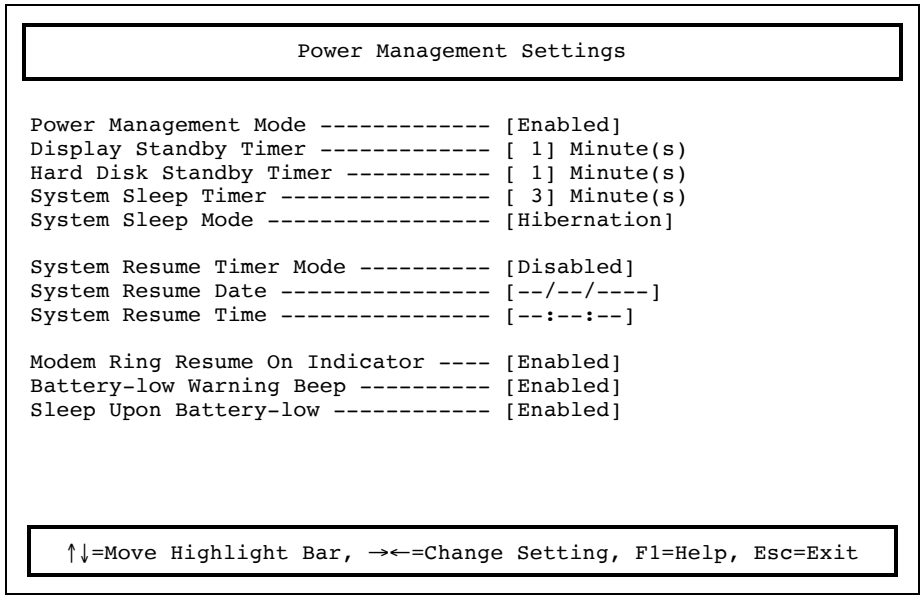
3.4.9 CardBus Support

The notebook comes pre-installed with a Windows 95 version which has built-in support for CardBus. In this case, CardBus Support is not needed and set to `[Disabled]`. If in case you install an older version of Windows 95 which does not have built-in Cardbus driver support, you need to enable this parameter. The default setting is `[Disabled]`.

To verify your Windows 95 version, access the System icon in the Control Panel. In the System section of the General tab, verify that the Windows 95 version is 4.00.950 B.

3.5 Power Management Settings

Besides accessing this screen from POST (**F2**), you can also press **Fn-F6** during runtime to access this section of Setup.



3.5.1 Power Management Mode

With enabled, all the timers in Setup take effect unless specifically disabled by the user. Select `[Disabled]` to turn off all the timers. The default setting is `[Enabled]`.

You cannot disable this parameter in Setup if APM is installed under DOS, Windows or Windows 95. To disable APM, type `Power Off` under DOS, or disable the Power icon in the Windows Control Panel.

3.5.2 Display Standby Timer

The notebook shuts off the LCD backlight and turns off the CRT video as well, if there is no activity from the keyboard or external PS/2 mouse within the period specified by this timer. To turn the display back on, press a key or move the mouse.

The valid values for this timer range from 1 to 15 minutes with default set at `[1]`. Select `[Off]` to disable the timer.

3.5.3 Hard Disk Standby Timer

The hard disk drive enters standby mode if there are no disk read/write operations within the period specified by this timer. The hard disk returns to normal mode once the notebook accesses it.

The valid values for this timer range from 1 to 15 minutes with default set at [1]. Select [Off] to disable the timer.

3.5.4 System Sleep Timer

This parameter enables you to set a timeout period for the notebook to enter either standby or hibernation mode. The System Sleep Mode parameter determines which sleep mode the notebook will enter into.

The valid values for this timer range from 1 to 15 minutes with default set at [3]. Select [Off] to disable the timer.

3.5.5 System Sleep Mode

This parameter tells the notebook which sleep mode (Standby or Hibernation) to enter into when the System Sleep Timer times out. The default setting is [Hibernation].

3.5.6 System Resume Timer Mode

When enabled, the notebook resumes from standby mode at the specified Resume Date and Resume Time parameter settings.

When the notebook is in hibernation mode, it cannot resume when this parameter is enabled.

3.5.7 System Resume Date and Time

The Resume Date and Resume Time parameters let you set the date and time for the resume operation. The date and time fields take the same format as the System Date and Time parameters in the Basic System Settings screen.

Setting a resume date and time that is not valid automatically disables these fields. A successful resume occurring from a date and time match automatically disables these fields.

3.5.8 Modem Ring Resume On Indicator

When enabled, the notebook wakes up from standby mode and returns to normal mode when a PCMCIA modem detects a ringing tone. The default setting is [Enabled].

When the notebook is in hibernation mode, it cannot resume from a modem ring.

3.5.9 Battery-low Warning Beep

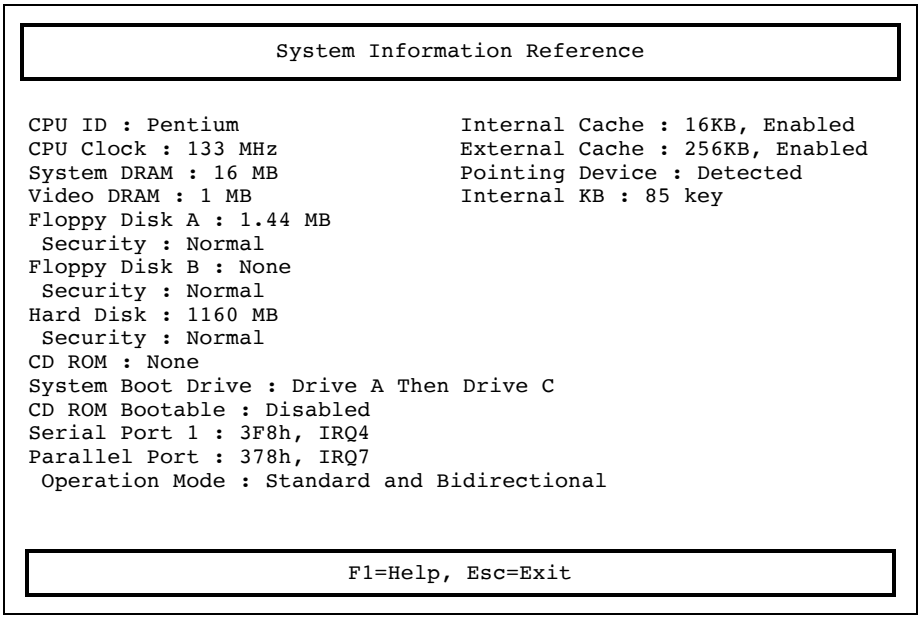
This parameter allows you to enable or disable the warning beep generated by the notebook when a battery-low condition occurs. The default setting is `[Enabled]`.

3.5.10 Sleep Upon Battery-low

This parameter enables the notebook to enter standby or hibernation mode when a battery-low condition takes place. The default setting is `[Enabled]`.

3.6 System Information Reference

If you access Setup during runtime (**Fn-F6**), pressing **PgDn** after the Power Management Settings screen displays a summary of your notebook's components and settings.



The items in this screen are not user-configurable. See table below.

Table 3-6 System Status Descriptions

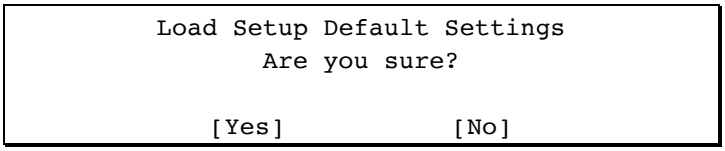
Item	Description
CPU ID	Shows the processor type
CPU Clock	Shows the processor speed
System memory	Shows the total system memory
Video memory	Shows the total video memory
Floppy Disk A	Shows the floppy drive A type
Security	Shows floppy drive A security setting
Floppy Disk B	Shows the floppy drive B type
Security	Shows floppy drive B security setting
Hard Disk	Shows the IDE drive type and size and its security setting
Security	Shows hard disk drive security setting
CD ROM	Shows the presence of a CD-ROM drive
System Boot Drive	Shows the boot sequence setting
CD ROM Bootable	Shows if the CD ROM Bootable feature is enabled or not
Serial Port 1	Shows the serial port base address and IRQ
Parallel Port	Shows the parallel port base address and IRQ
Operation Mode	Shows the parallel port operation mode
Internal Cache	Shows the internal cache size and setting
External Cache	Shows the external cache size
Pointing Device	Shows the presence of a pointing device
Internal KB	Shows the internal keyboard type

This screen may show other items which are not in this list if certain parameters settings are changed and enabled.

3.7 Load Setup Default Settings

Selecting this option allows you to load all the default settings. The default settings are the values initially stored in CMOS RAM intended to provide high performance. If in the future, you change these settings, you can load the default settings again by selecting this option.

When you select this option, the following prompt appears:



Select `[Yes]` to load the default settings or `[No]` to abort the operation.

Disassembly and Unit Replacement

This chapter contains step-by-step procedures on how to disassemble the notebook computer for maintenance and troubleshooting.

To disassemble the computer, you need the following tools:

- Wrist grounding strap and conductive mat for preventing electrostatic discharge
- Flat-bladed screwdriver
- Phillips screwdriver
- Hexagonal screwdriver
- Tweezers
- Plastic stick

The screws for the different components vary in size. During the disassembly process, group the screws with the corresponding components to avoid mismatch when putting back the components.

4.1 General Information

4.1.1 Before You Begin

Before proceeding with the disassembly procedure, make sure that you do the following:

1. Turn off the power to the system and all peripherals.
2. Unplug the AC adapter and all power and signal cables from the system.
3. Remove the battery pack from the notebook by (1) pressing the battery compartment cover release button, and sliding out the cover. Then (2) pull out the battery pack.

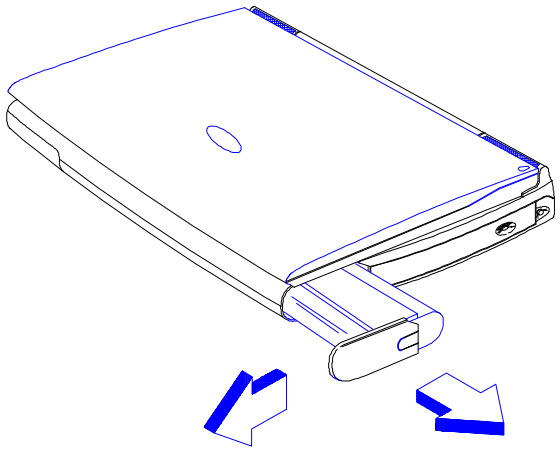


Figure 4-1 Removing the Battery Pack

Removing all power sources from the system prevents accidental short circuit during the disassembly process.

4.1.2 Connector Types

There are two kinds of connectors on the main board:

- Connectors with no locks

  Unplug the cable by simply pulling out the cable from the connector.

- Connectors with locks

  You can use a plastic stick to lock and unlock connectors with locks.

The cables used here are special FPC (flexible printed-circuit) cables, which are more delicate than normal plastic-enclosed cables. Therefore, to prevent damage, make sure that you unlock the connectors before pulling out the cables. Do not force cables out of the connectors.

CONNECTORS WITH LOCKS

- Unplugging the Cable

  To unplug the cable, first unlock the connector by pulling up the two clasps on both sides of the connector with a plastic stick. Then carefully pull out the cable from the connector.

- Plugging the Cable

  To plug the cable back, first make sure that the connector is unlocked, then plug the cable into the connector. With a plastic stick, press the two clasps on both sides of the connector to secure the cables in place.

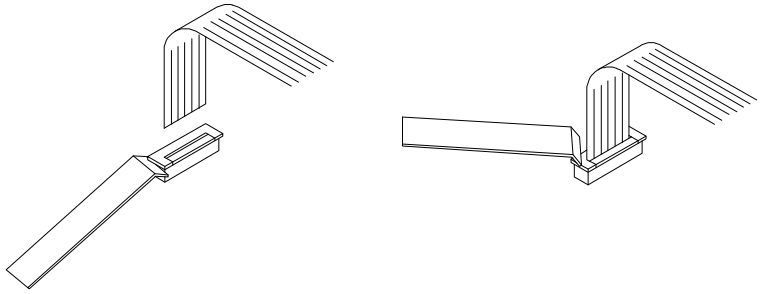


Figure 4-2 Using Connectors With Locks

Connectors mentioned in the following procedures are assumed to be no-lock connectors unless specified otherwise.

4.1.3 Disassembly Sequence

The disassembly procedure described in this manual is divided into four major sections:

- Section 4.2: Replacing Memory
- Section 4.3: Removing the hard disk drive
- Section 4.4: Removing the keyboard
- Section 4.5: Disassembling the inside frame assembly
- Section 4.6: Disassembling the display

The following table lists the components that need to be removed during servicing. For example, if you want to remove the motherboard, you must first remove the keyboard, then disassemble the inside assembly frame in that order.

Table 4-1 Guide to Disassembly Sequence

Service Item	Prerequisite
Remove or replace the hard disk drive	1. Remove HDD Door.
Remove or replace the internal module	1. Remove the keyboard. 2. Disassemble the housing
Remove the motherboard for service or replacement	1. Remove the keyboard. 2. Disassemble the housing.
Remove the touchpad	1. Remove the keyboard 2. Disassemble the housing
Replace the LCD	Remove the display
Install CPU	Remove the keyboard (and heat sink assembly)
Install additional memory	Remove DIMM cover

The flowchart on the succeeding page gives a clearer and more graphic representation on the entire disassembly sequence. Please refer to it from time to time.

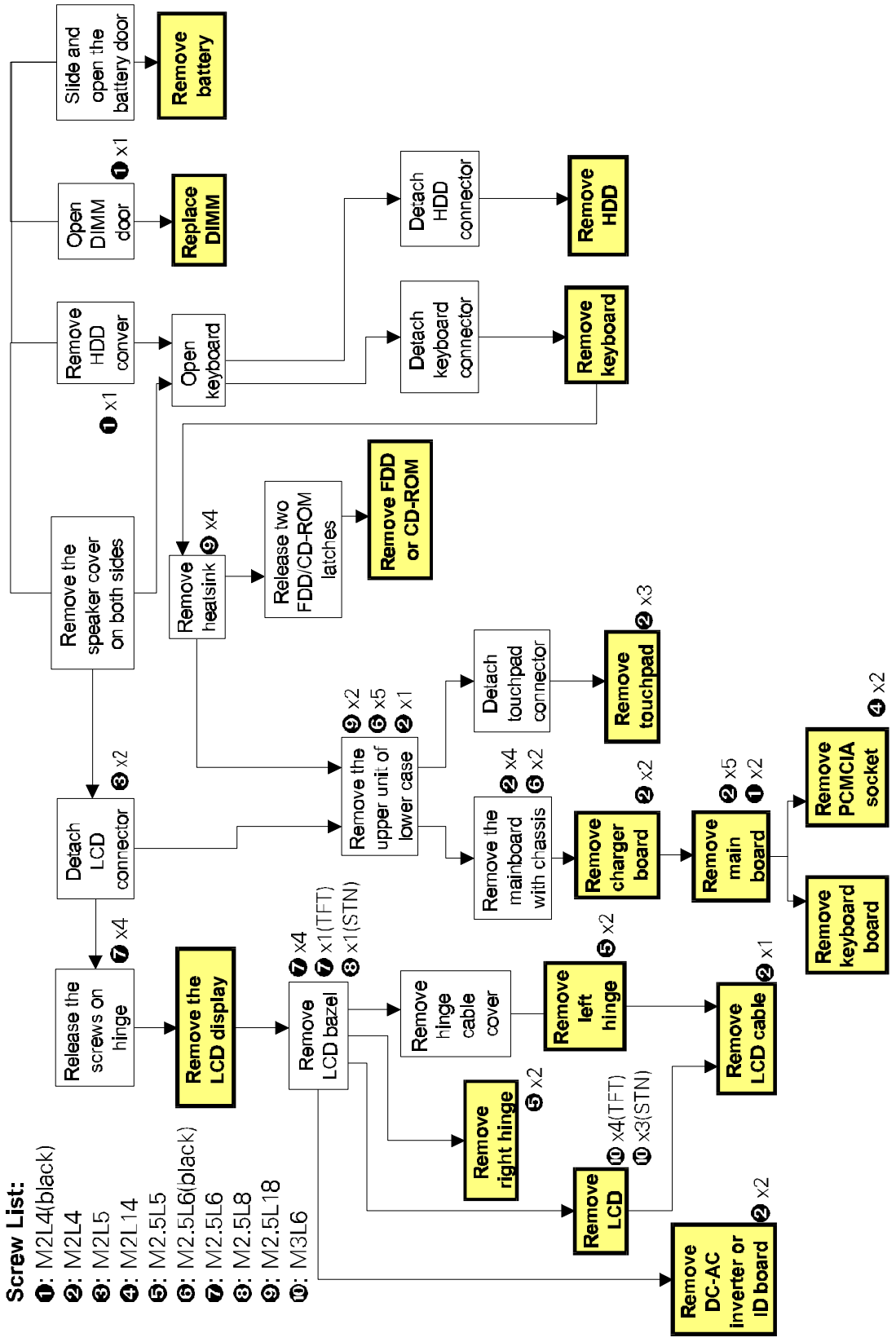


Figure 4-3 Disassembly Sequence Flowchart

4.2 Replacing Memory

Follow these steps to insert memory modules:

1. Turn the computer over to access the base.
2. Remove the screw from the memory expansion door and remove the door.

The memory door screw is part of the memory door and does not separate from the memory door.

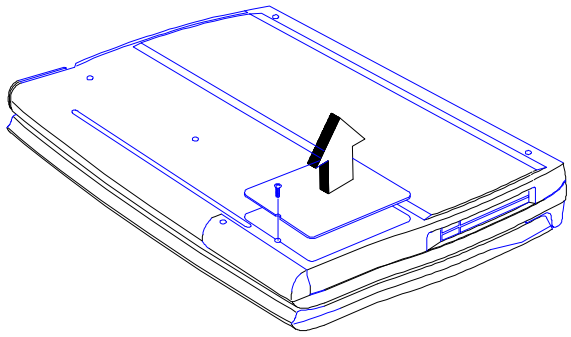


Figure 4-4 Removing the Memory Door

3. Remove the memory modules from its shipping container.
4. Align the connector edge of the memory module with the key in the connector. Insert the edge of the memory module board into the connector. Use a rocking motion to fully insert the module. Push downward on each side of the memory module until it snaps in place.

   To remove the memory module, release the slot locks found on both ends of the memory slot to release the DIMM. Then pull out the memory module.

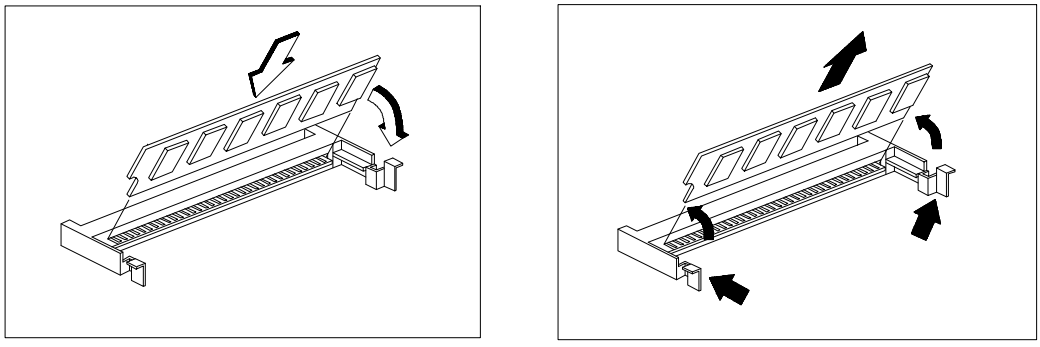


Figure 4-5 Installing and Removing Memory

5. Replace the memory expansion door and screw in place.

Sleep Manager must be run after installing additional memory for the computer to hibernate properly. If Sleep Manager is active, it will automatically adjust the hibernation file on your notebook.

If you are using an operating system other than Windows 95 or DOS, you may need to re-partition your hard disk drive to allow for the additional memory. Check with your system administrator.

4.3 Removing the Hard Disk Drive

Follow these steps to remove the hard disk drive:

1. Turn the computer over and locate the hard disk drive bay cover.
2. Remove the screw that secures the hard disk drive bay cover. Then slide out and remove the the cover. Set aside the cover.

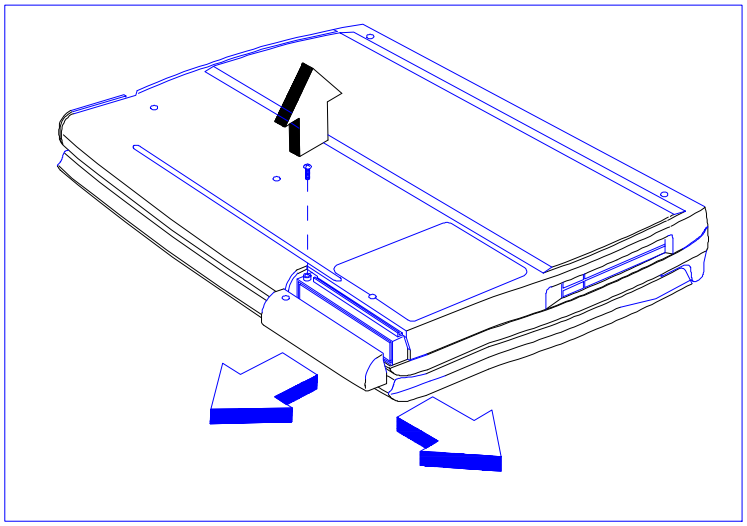


Figure 4-6 Removing the Hard Disk Drive Bay Cover

3. You will see a tape handle attached to the hard disk drive. Pull out the hard disk drive using the tape handle.

Be careful pulling the hard disk drive out. Make sure the connector of the hard disk drive transfer board doesn't loosen while removing the hard disk drive.

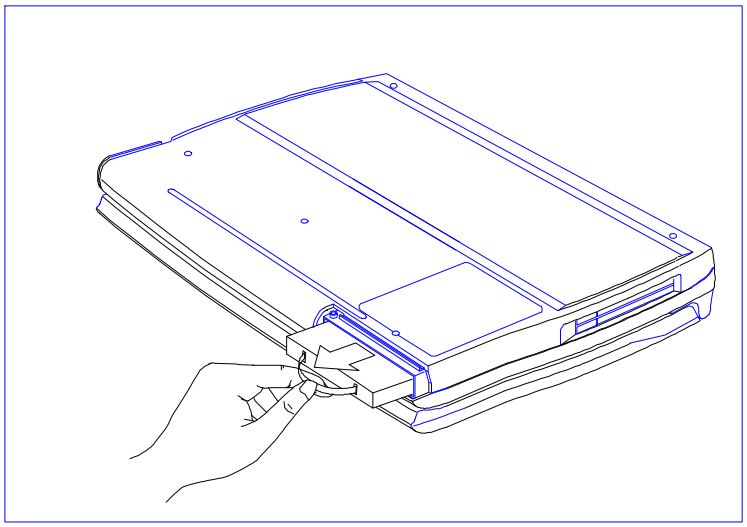


Figure 4-7 Removing the Hard Disk Drive

4. Store the hard disk drive in an antistatic bag.

If you want to install a new hard disk drive, reverse the steps described above.

4.4 Removing the Keyboard

Follow these steps to remove the keyboard:

1. Slide out (1) and pull up (2) the two display hinge covers on both sides of the notebook.

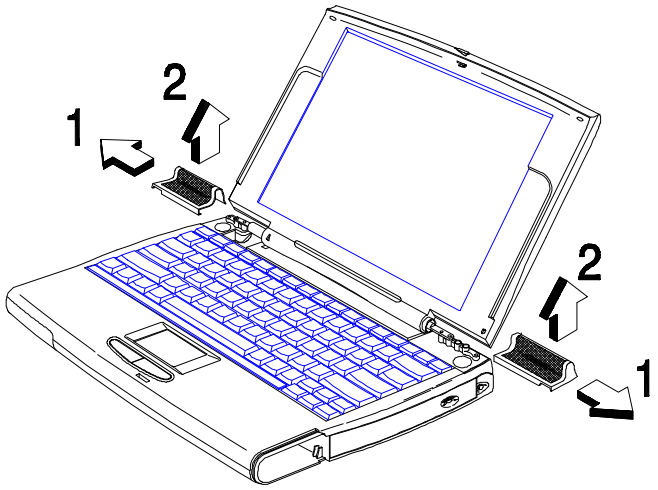


Figure 4-8 Removing the Display Hinge Covers

2. Unplug the keyboard connectors (CN1 and CN2) from the keyboard connection board. Set aside the keyboard.

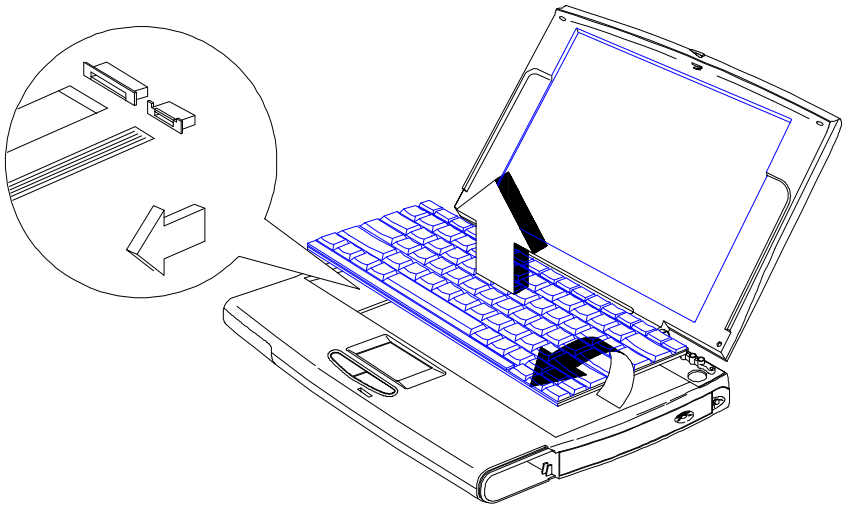


Figure 4-9 Unplugging the Keyboard Connectors

4.5 Disassembling the Inside Frame Assembly

This section discusses how to disassemble the housing, and during its course, includes removing and replacing of certain major components like the internal drive (CD-ROM or floppy), CPU and the main board. Follow these steps:

4.5.1 Removing the Heat Sink Assembly

Remove the four screws that secure the heat sink to the housing.

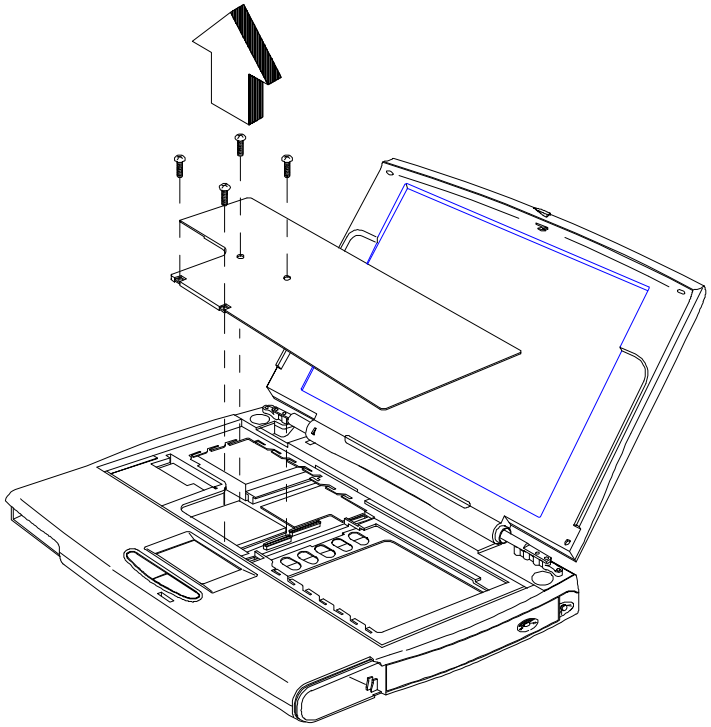


Figure 4-10 Removing the Heat Sink Assembly Screws

4.5.2 Removing the Internal Drive

1. Pull up and remove the FDD/CD module latches.
2. Unplug the internal drive cable (CN14/CN17 for CD-ROM or CN14 for FDD).
3. Pull out the internal drive and set it aside.

Ensure the drive cables do not become hooked on the inside frame assembly when removing and reinstalling the drive.

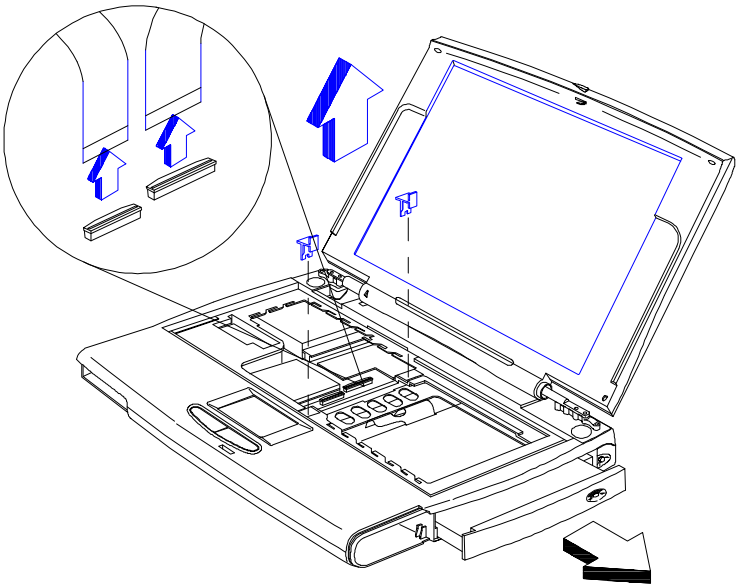


Figure 4-11 Removing the Internal Drive

4.5.3 Replacing the CPU

The unique ZIF (zero insertion force) socket allows you to easily remove the CPU. Follow these steps to remove the CPU and install a replacement CPU. See figure below.

1. Insert a flat-blade screwdriver into the opening at the left end of the socket (labeled OPEN) and push towards the other end of the socket.

2. Pull out the CPU. Then insert the replacement CPU. Insure the CPU is properly keyed before pressing it into the socket.

3. Insert a flat-blade screwdriver into the opening at the right end of the socket (labeled LOCK) and push towards the other end of the socket.

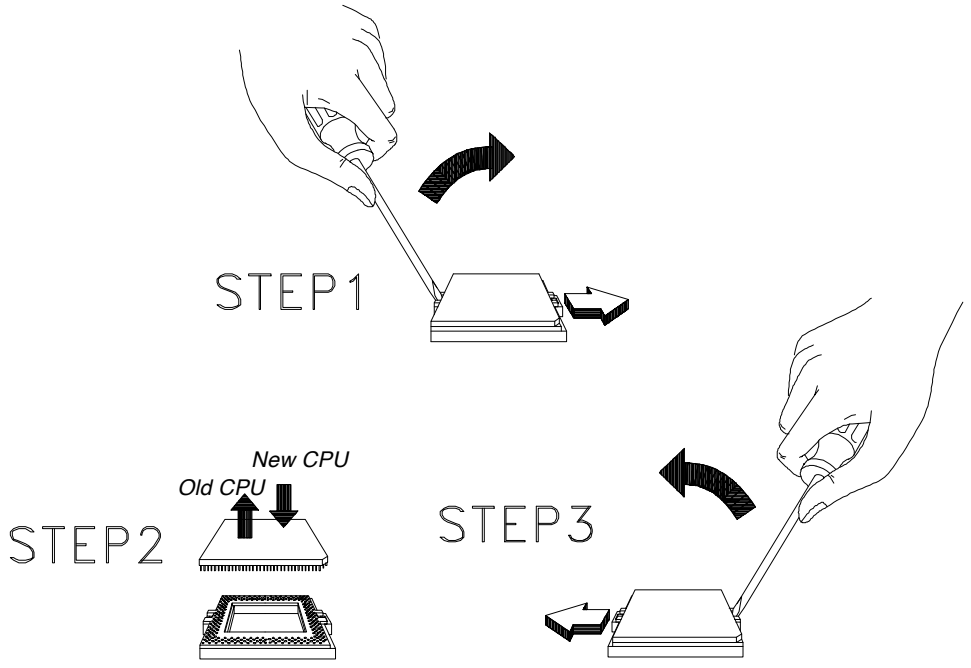


Figure 4-12 Replacing the CPU

4.5.4 Removing the Display

1. Remove the two screws that secure the display cable to the motherboard. Then unplug the display cable.

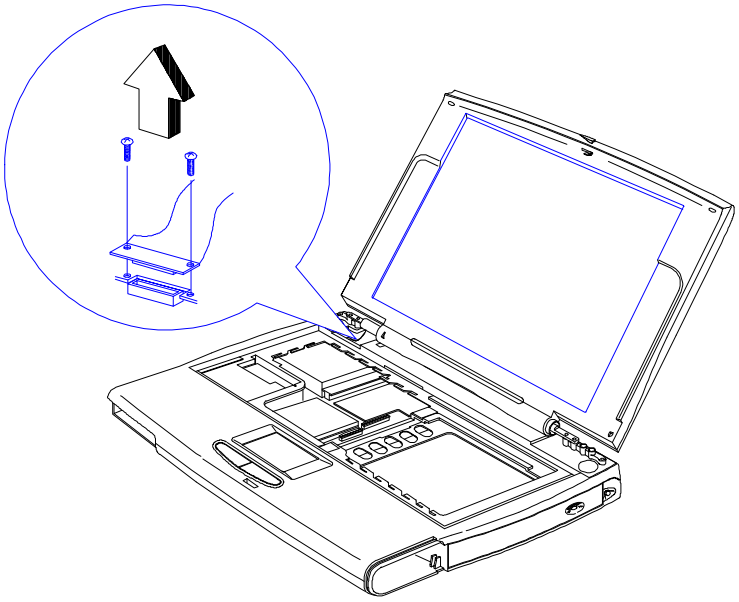


Figure 4-13 Unplugging the Display Cable

2. Remove the four display hinge screws. Then detach the display from the main unit and set aside.

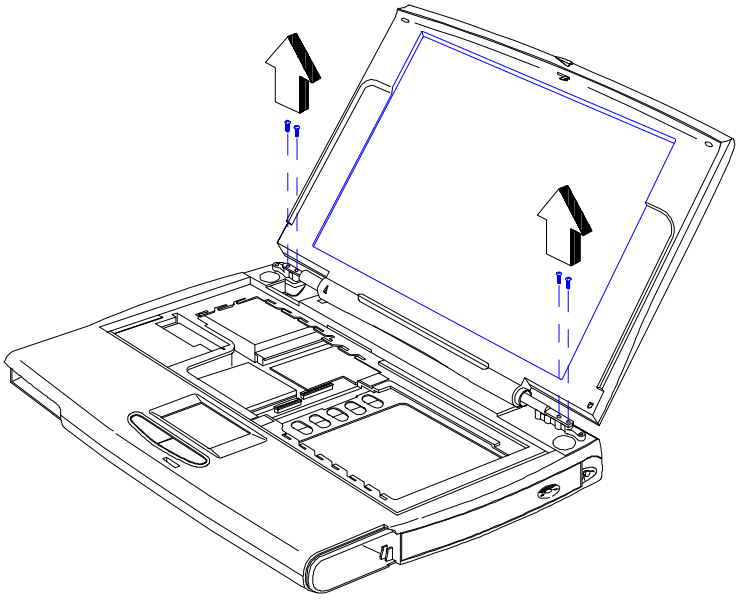


Figure 4-14 Removing the Display Hinge Screws

4.5.5 Detaching the Top Cover

1. Screws found on the lower case secure the top cover with the lower. However, you may not need to remove all six screws. Follow the discussion below for details.
   - If you only want to remove the top cover from the lower case, remove all screws except for the encircled ones in this figure below.
   - If you intend to remove the motherboard with the chasis from the lower case, remove all screws.

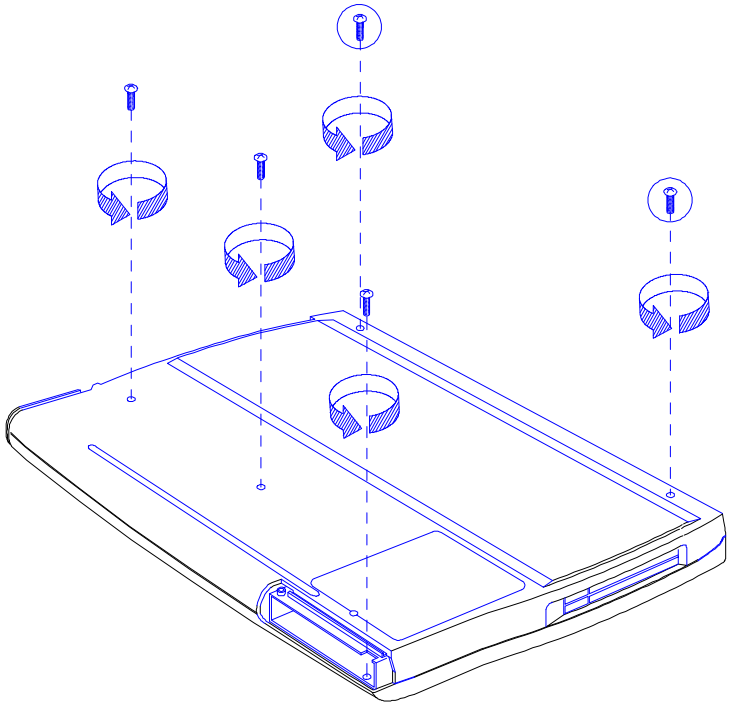


Figure 4-15 Removing the Bottom Screws

2. Remove three screws near the display hinge screw holes and one screw near the PC card slots. Before you detached the top cover make sure that you unplug the cable for the CN19 (touch pad). Unsnap the top cover from the base assembly and set aside.

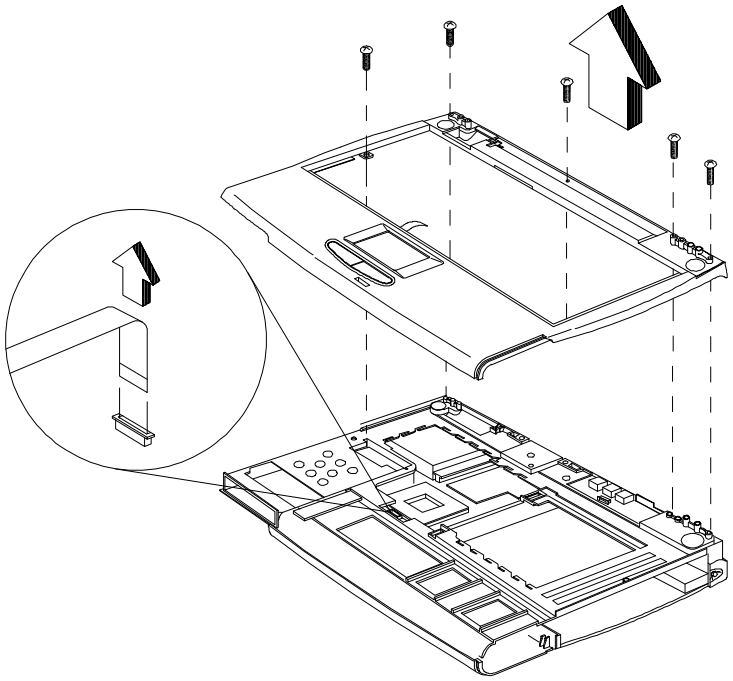


Figure 4-16 Detaching the Top Cover from the Base Assembly

4.5.6 Removing the Base Assembly

Remove four screws that secure the inside frame assembly to the base assembly. Then detach the inside frame assembly from the base assembly.

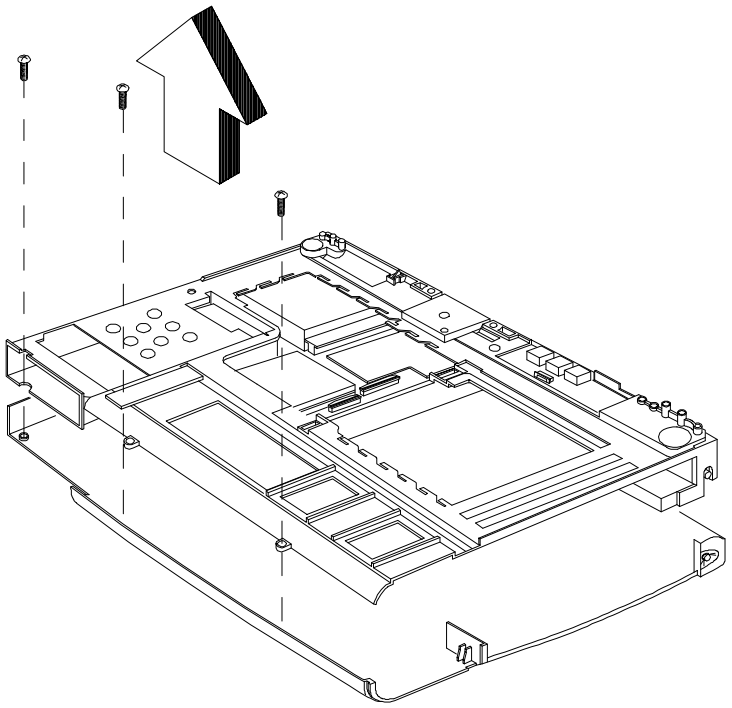


Figure 4-17 Detaching the Base Assembly

4.5.7 Removing the Motherboard

1. Remove the fan by (3) removing the sticker and (4) unplugging the fan cable (CN9).

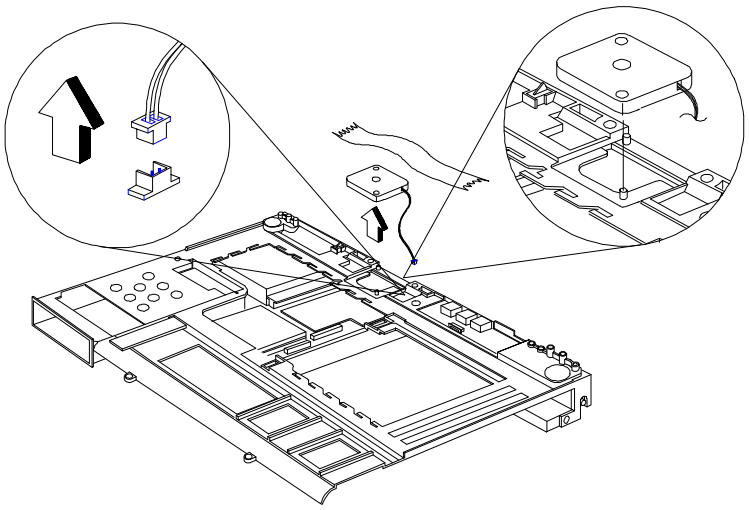


Figure 4-18 Removing the Fan

When installing the fan, the fan hole should face the rear of the unit to draw thermal air out of the system.

2. Remove the audio board by (1) unplugging the audio board connector (CN5), and then (2) pulling up the audio board.

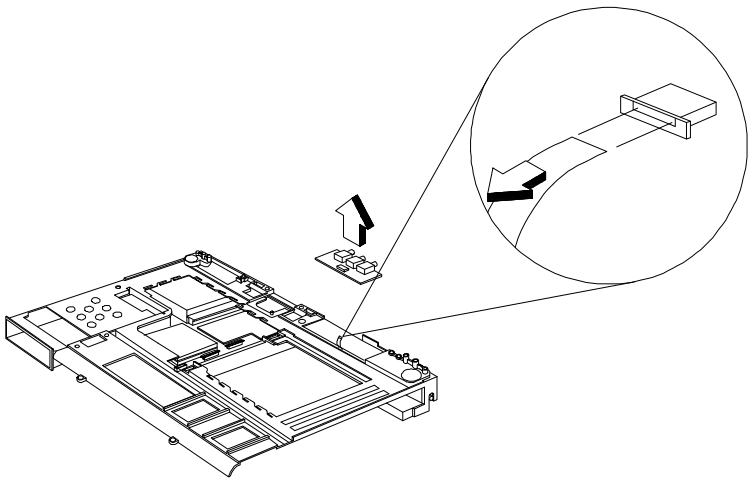


Figure 4-19 Removing the Audio Board

3. Unplug the battery connector board cable (CN18).

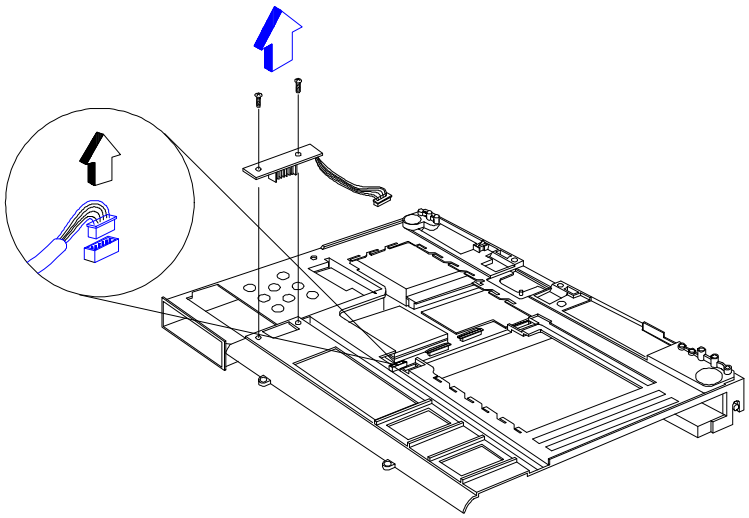


Figure 4-20 Removing the Battery Connector Board

4. Unplug the (a) LCD cover switch cable (CN8) and (b) speaker cables (CN7 and CN10).

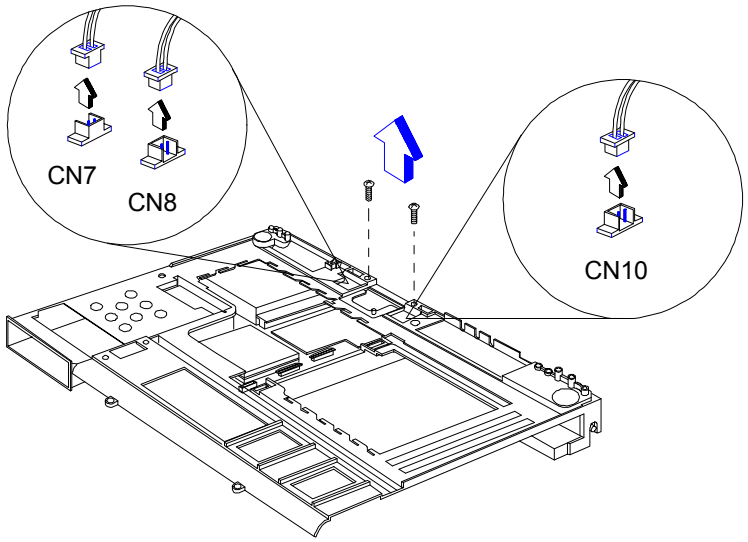


Figure 4-21 Unplugging the LCD Cover Switch and Speaker Cables

5. Turn the unit over and remove the two screws that secure the Charger Board to the inside of the assembly frame. Then remove the board.

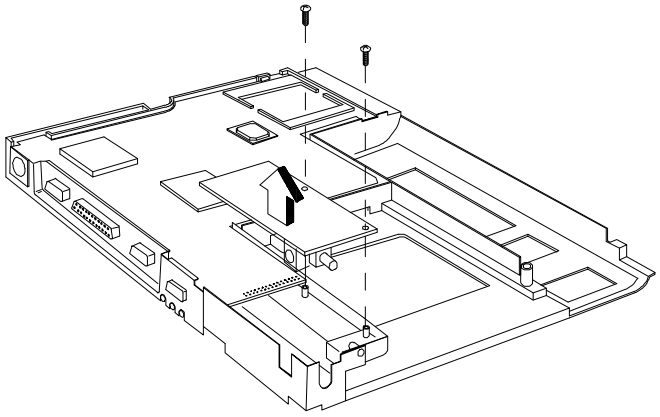


Figure 4-22 Removing the Charger Board

6. Remove seven screws that secure the motherboard to the inside assembly frame. Then release the latch and pull up the motherboard to detach it from the inside assembly frame.

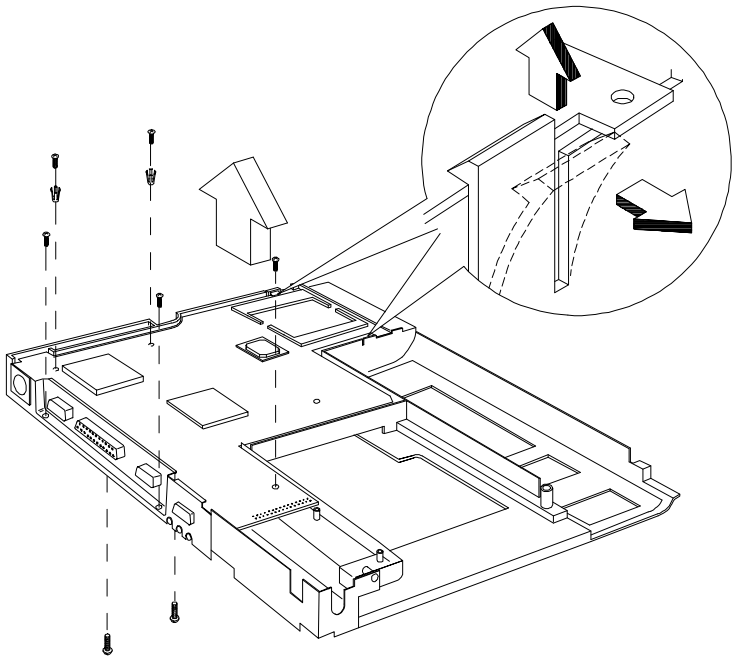


Figure 4-23 Detaching the Motherboard from the Inside Assembly Frame

4.5.8 Disassembling the Motherboard

REMOVING THE PC CARD SLOT UNIT

The PC Card Connector Module is normally part of the motherboard spare part. The following removal procedure is for reference only.

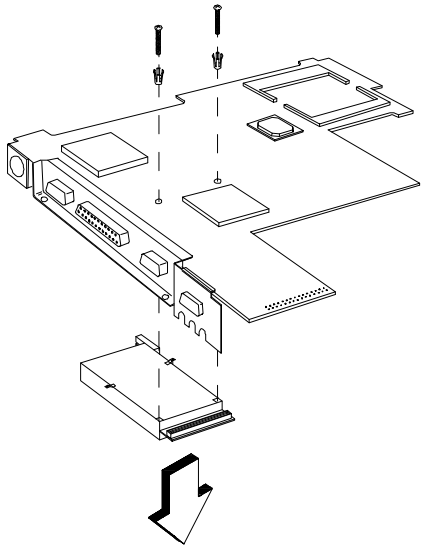


Figure 4-24 Removing the PC Card Slot Unit

REMOVING THE KEYBOARD CONNECTION BOARD

Pull up the keyboard connection board to remove it.

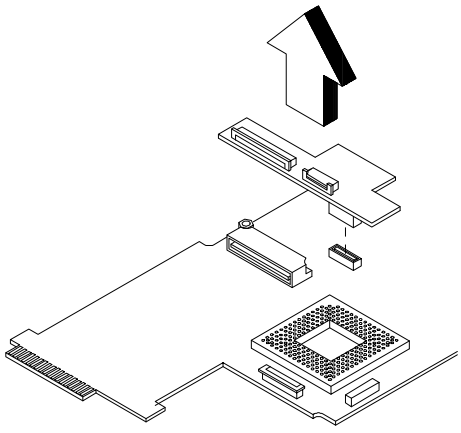


Figure 4-25 Removing the Keyboard Connection Board

4.5.9 Removing the Touchpad

The touchpad is connected to the top cover. Follow these steps to remove the touchpad assembly:

1. Peel off the mylar.
2. Remove the three screws and disconnect the touchpad cable (J2), then remove the touchpad main sensor and connector unit.
3. Lift up and remove the touchpad.
4. Lift up and remove the touchpad buttons.

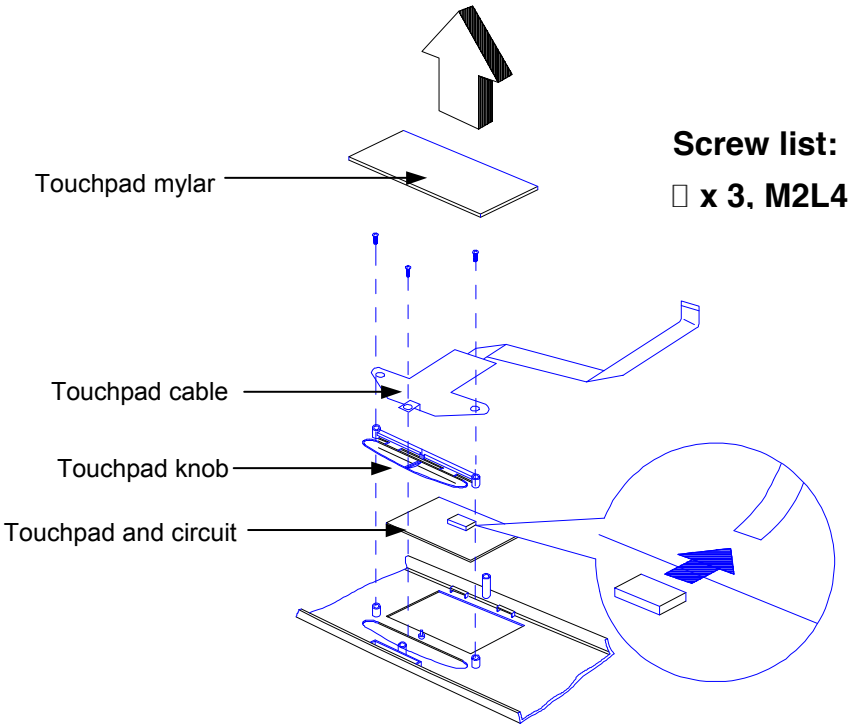


Figure 4-26 Removing the Touchpad

4.6 Disassembling the Display

Follow these steps to disassemble the display:

1. Remove the oval LCD bumpers at the top of the display and the long bumper on the LCD hinge.

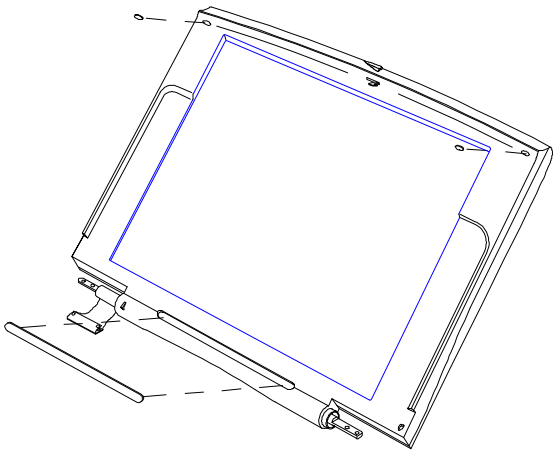
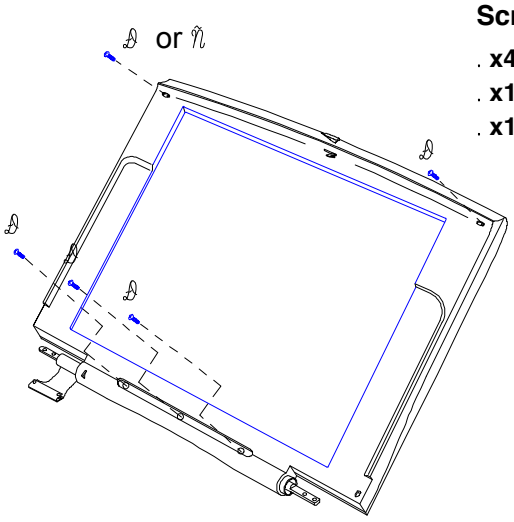


Figure 4-27 Removing the LCD Bumpers

2. Remove five screws on the display bezel.



Screw List:

. **x4, M2.5L6**
. **x1, M2.5L6(for 11.3” TFT LCD)**
. **x1, M2.5x8(for 11.3” STN and 12.1” TFT LCD)**

Figure 4-28 Removing the Display Bezel Screws

STN and TFT LCDs use the same bezel but different panels.

3. Pull out and remove the display bezel by first pulling on the inside of the bezel sides and lower bezel area. Then pull up the top bezel area.

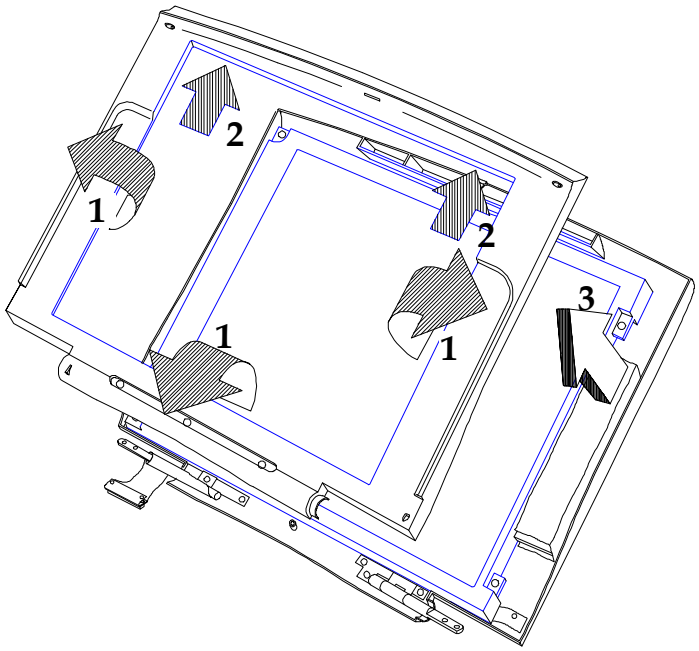


Figure 4-29 Removing the Display Bezel

4. Twist (1), then slide out (2) and remove the Hinge Cable Cover.

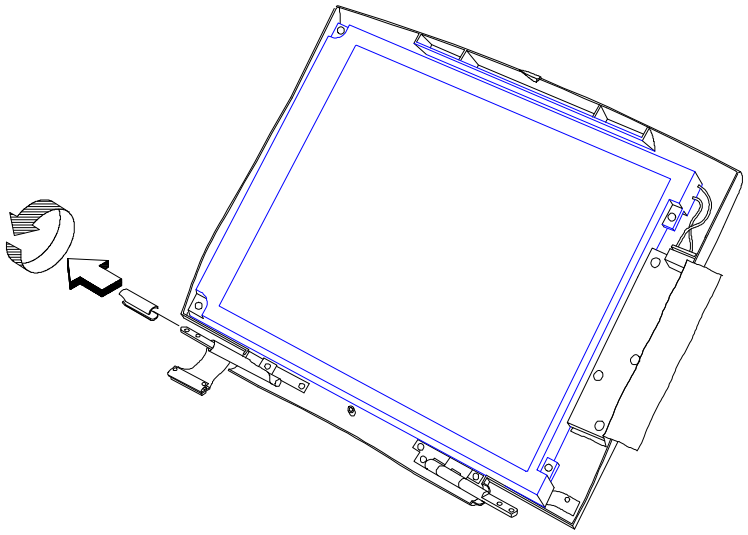


Figure 4-30 Removing the Hinge Cable Cover

The hinge cable cover cannot be removed unless the LCD bezel is removed.

5. Remove screws on the four sides of the display panel. Then gently fold back the foil around the display panel and unplug the inverter cable (J2).

The encircled screw doesn't exist in STN LCD model .

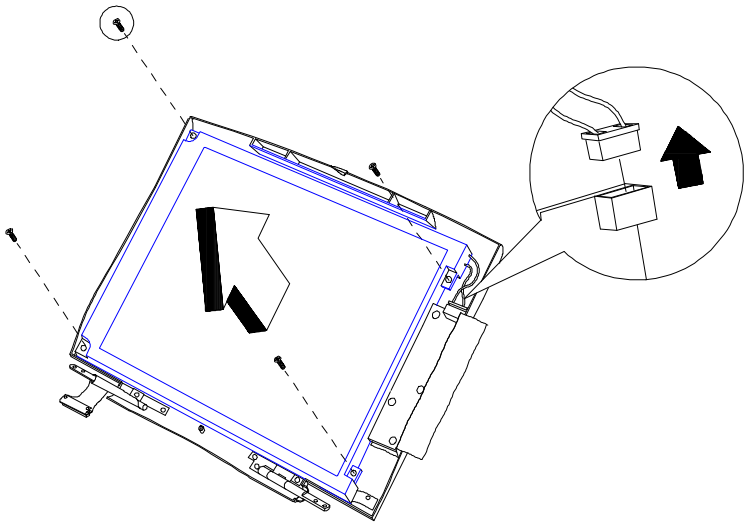


Figure 4-31 Removing the LCD Panel

6. Tilt the LCD Panel away for the display cover. Then unplug the LCD Panel from the Display Cable Assembly.

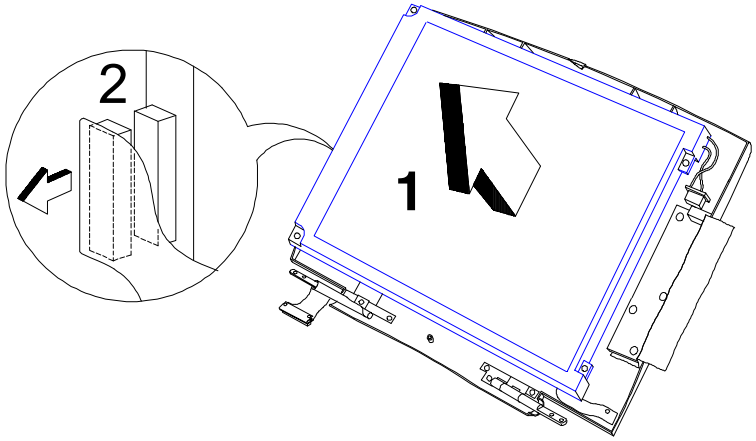


Figure 4-32 Removing the LCD

5. Remove the screws that secure the DC-AC Inverter Board to the display back cover and remove the inverter boards. Then unplug the display cable.

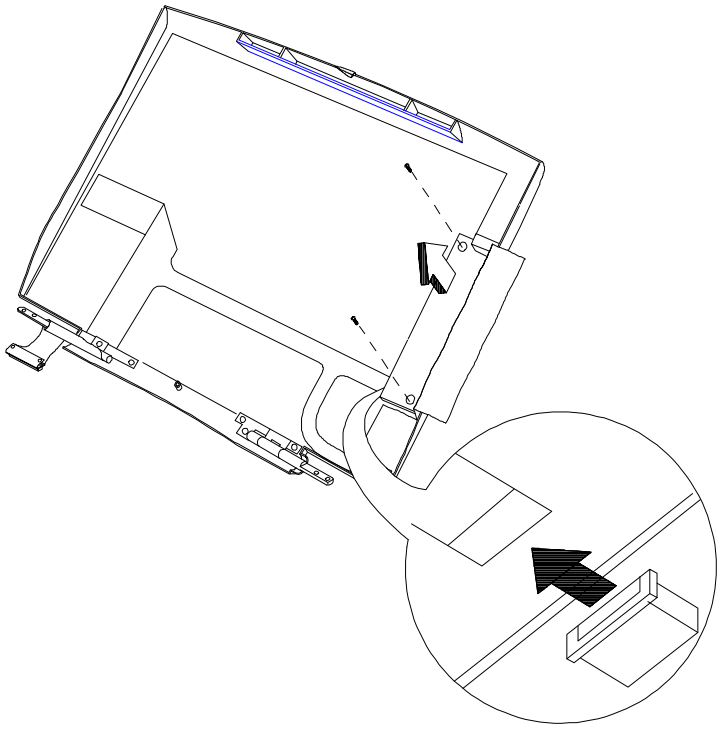
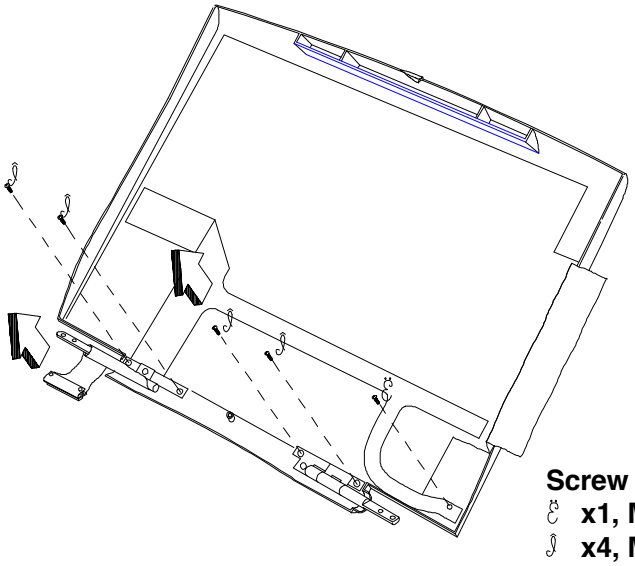


Figure 4-33 Removing the DC-AC Inverter and LCD ID Inverter Boards

5. Remove five screws that secure the LCD cable to the display back over, then remove the LCD cable assembly.



Screw list:
x1, M2L4
x4, M2.5L5

Figure 4-34 Removing the Display Cable Assembly

Model Number Definition

This appendix shows the model number definition of the notebook.

610XX-X X X

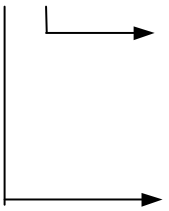
Keyboard Language Version

0: Swiss/US	G: German
1: US(110V)	I: Italian
2: US(220V)	J: Japanese
3: US w/o power cord	N: Norwegian
4: US K/B w/o power cord(ACLA)	R: Russian
5: US(110V for AAB)	S: Spanish(220V)
6: US(220V)with CCIB for P.R. Chinese	T: Thailand
7: Spanish w/o power cord	U: UK(250V)
8: Turkish	W: Swedish/Finnish
A: Arbic	S: Swiss/German
C: Chinese	Y: Swiss/French
D: Danish	K: Korean
F: French	Z: w/o Keyboard

Memory and Battery

0: Li-Ion BTY+CD-ROM+W/O CPU
1: NiMH BTY+CD-ROM+W/O CPU
2: NiMH BTY+FDD+W/O CPU
3: Li-Ion BTY+FDD+W/O CPU
4: Intel 150MHz CPU+Li-Ion BTY+CD-ROM+16MB
5: Intel 150MHz CPU+Li-Ion BTY+CD-ROM+16MB+Generic
6: Intel 133MHz CPU+Li-Ion BTY+CD-ROM+16MB
7: Intel 133MHz CPU+Li-Ion BTY+CD-ROM+16MB+Generic
8: Intel 120MHz CPU+NiMH BTY+FDD+8MB
9: Intel 120mhz CPU+NiMH BTY+FDD+16MB
A: Intel 120mhz CPU+NiMH BTY+FDD+8MB+Generic
B: Intel 133MHz CPU+NiMH BTY+FDD+8MB
C: Intel 133MHz CPU+NiMH BTY+FDD+16MB
D: Intel 133MHz CPU+NiMH BTY+FDD+16MB+Generic
E: W/O CPU+Li-Ion BTY+CD-ROM(bulk pack)
F: W/O CPU+NiMH BTY+CD-ROM(bulk pack)
G: W/O CPU+NiMH BTY+FDD(bulk pack)
H: W/O CPU+Li-Ion BTY+FDD(bulk pack)
I: W/O CPU+W/O BTY+0MB RAM(bulk pack)
J: Intel P55C 133MHz CPU+Li-Ion BTY+CD-ROM+16MB
K: Intel P55C 133MHz CPU+NiMH BTY+CD-ROM+16MB
L: Intel P55C 150MHz CPU+Li-Ion BTY+CD-ROM+16MB
M: Intel P55C 150MHz CPU+CD-ROM+16MB RAM(4 in 1 bulk pack)
N: Intel 150MHz CPU+FDD+16MB RAM(4 in 1 bulk pack)
O: Intel 150MHz CPU+CD-ROM+16MB RAM(4 in 1 bulk pack)
P: Intel 150mhz CPU+FDD+Li-Ion BTY+8MB
Q: Intel 150mhz CPU+CD-ROM+NiMH BTY+16MB RAM
R: Intel 133mhz CPU+CD-ROM+16MB RAM(bulk pack)
S: Intel 120CPU,16MB RAM+FDD+Li-Ion BTY
T: Intel 133 +NiMH BTY+CD-ROM+16MB MEMORY
U: Intel 133+NiMH BTY+CD-ROM+16MB MEMORY(GENERIC)
V: Intel 120+NiMH BTY+CD-ROM+16MB MEMORY
W: Intel P55C 150MHz CPU+CD-ROM+24MB RAM(4 in 1 bulk pack)
X: Intel P55C 150MHz CPU+CD-ROM+32MB RAM(4 in 1 bulk pack)

370PXX-X X X



Hard Disk

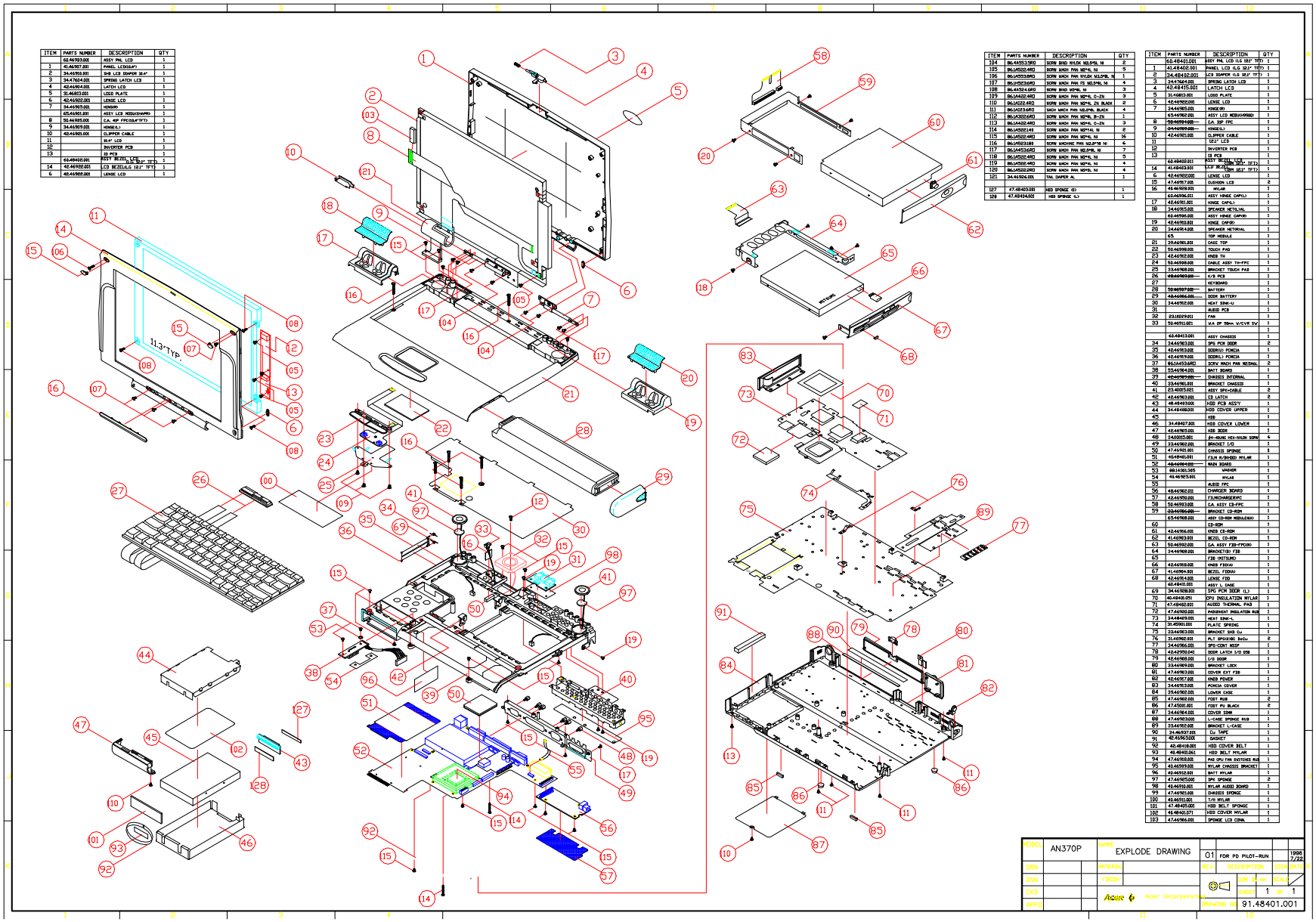
0: No Hard Disk	3:340MB	A: 1GB
1: 120MB	5:520MB	C:1.35GB
2: 200MB	8:810MB	D:1.4GB
B: 250MB	9:1.3GB	E: 2.1GB

LCD

C :11.3" DSTN
CX:11.3" TFT
DX:12.1" TFT

Exploded View Diagram

This appendix shows an exploded view diagram of the notebook.


AN370P
EXPLODE DRAWING
91.48401.001

Spare Parts

This appendix lists the spare parts of the notebook TI EXTENSA 610.

Table C-1 Spare Parts List

	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
<< MECHANICAL & MODULES >>					
1	IC CHARGE (power supply charger bd)	05.62062.020	9811768-0001	56	
2	FAN 5V UDQFC3E09 105MM	23.10029.011	9811769-0001	32	
3	ADT (AC Adapter w/o power cord)	25.10052.001	9811770-0001		see options for AC adapter with cord
4	HEAT SINK-U(2) AL AN370	34.46925.001	981177100001	30	
5	CASE UPPER (TOP) 370P/TI	39.46901.031	9811772-0001	21	w/o label
6	C.A FPC TOUCH PAD 370P	6M.48415.001	9811774-0001	24, 25	w/cable, bracket
7	C.A FPC AUDIO BD 370P	50.48402.001	9811775-0001		
8	HDD 1083MB TOSHIBA/MK1002MAV	56.02775.001	9811776-0001		without case or cable
9	HDD 1440MB HIT-DK225A-14	56.02568.031	9815585-0001		
10	HDD 2160MB IBM/DTNA -22160	56.02941.011	9815586-0001		
11	HDD TRANSFER BD	55.48403.001	9811802-0001		w/ connector
12	ASSY HDD UPPER COVER	60.48412.101	9811783-0001	44	w/mylar
13	ASSY HDD LOWER COVER	60.48418.101	9811785-0001	46	w/mylar, belt sponge
14	TOUCHPAD SYNAP/TM1202MPU-156-1	56.17450.011	9811777-0001	22	w/o label
15	ASSY HINGE (COVER) CAP(R) 050 AN370	60.46906.001	9811778-0001	7	w/net speaker, hinge cap
16	ASSY HINGE (COVER) CAP(L) 050 AN370	60.46906.011	9811779-0001	10	w/net speaker, hinge cap
17	ASSY LOWER CASE (BASE) 370P	60.48411.001	9811782-0001		w/bracket, pcmcia cover, I/o door, knob power, foot rub, cover ext FDD, simm cover
18	ASSY CHASSIS AN370P	60.48413.001	9811784-0001		w/speaker, battery bd, PCMCIA door, mylar, cover switch
19	FDD EXTERNAL 370	91.46905.012	9811788-0001		w/cable
20	ASSY CD-ROM KIT (V32)	91.46928.023	9811789-0001		w/bracket, cable, bezel, knob
21	C.A. ASSY CD-FPC,EXT 61X	50.46903.002	9815582-0001	58	
22	CD-ROM BEZEL	41.46903.001	9815587-0001		

Table C1 Spare parts list (continued)

	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
<< DISPLAY COMMON PARTS >>					
1	HINGE (L), SAE AN370, EXT 61X	34.46909.001	9813520-0001		
2	HINGE (R), EXT. 61X	34.46905.001	9811814-0001		
3	MYLAR, LCD, 100MM, EXT 61X	40.46928.001	9811817-0001		
4	LCD LATCH, EXT 61X	6M.48410.001	9815579-0001	3, 4	w/ spring
<< LCD KIT (STN) >> Hitachi 11.3"					
1	INVERTER T62.064.C.00 370P	19.21030.101	9811790-0001	12	
3	C.A 31P FPC 11.3"STN 370(W.C)	6M.48412.001	9811791-0001	1,2	w/ tail diaper
4	(LCD PANEL) LCDM LMG9900 11.3 STN SVGA HIT	56.07355.011	9811792-0001	1	
5	ASSY LCD BEZEL(11.3")050 370P	60.46902.101	9811793-0001	14	w/lens
6	COVER ASSY LCD(11.3 HI) 050 370PT	60.48401.151	9811794-0001		w/lens, diaper, assy latch, hinge(R); no TI logo
<< LCD KIT (STN) >> Sanyo 11.3"					
1	COVER ASSY LCD PNL	60.48401.151	9811794-0001	1	w/lens, diaper assy., latch, hinge(R), no TI logo
2	ASSY C.A 31P FPC 11.3" STN 370	6M.48412.001	9811791-0001	1,2	w/ tail diaper
3	(LCD PANEL)LCDM (sanyo 11.3" DSTN)	56.07469.001	9815588-0001		
4	ASSY LCD BEZEL(11.3") 050 370P	60.46902.101	9811793-0001	14	W/LENS
5	INVERTER BD	19.21030.101	9811790-0001	12	
<< LCD KIT (TFT) >> LG 12.1"					
1	COVER ASSY LCD PNL	60.48401.171	9815589-0001	1	w/lens, diaper assy., latch, hinge(R), no TI logo
2	ASSY C.A FPC, LG 12.1	6M.48414.001	9815591-0001	1,2	w/ tail diaper
3	LCDM LP 121S 12.1"(LCD PANEL)	56.07530.011	9815590-0001		
4	ASSY LCD BEZEL	60.48402.001	9815592-0001	14	W/LENS
5	INVERTER BD	19.21030.081	9815593-0001	12	
<< LCD KIT (TFT) >> 11.3" IBM					
1	INVERTER T62.064.C.00 370P	19.21030.101	9811790-0001	12	
2	C.A FPC 11.3TFT/SHARP 370(W.C)	50.46917.021	9811795-0001	1,2	w/ tail diaper
3	(LCD PANEL) LCM ITSV45E 11.3"TFT SVGA IBM	56.07469.101	9811796-0001		
4	ASSY LCD BEZEL(11.3")050 370P	60.46902.101	9811793-0001	14	w/ lens
5	COVER ASSY LCD PNL(11.3TFT)IBM 370PTI	60.48401.161	9811797-0001	1	w/lens, diaper, latch assy., hinge(R); and no TI logo

Table C1 Spare parts list (continued)

	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
<< MAIN BD >>					
1	IC CPU INTEL P54CSLM 120M 3.1V	01.IP54S.C0M	9811798-0001		
2	IC CPU INTEL P54CSLM 150M 2.9V SPGA	01.IP54S.F0B	9815594-0001		
3	IC CPU INTEL P55C (MMX) 150M 2.45V SPGA	01.ip55c.f00	9815595-0001		
4	MAIN BOARD 0MB W/O CPU 370P	55.48401.001	9811800-0001		w/o CPU
5	AUDIO BOARD 370P	6M.48417.001	9811801-0001	31	audio bd & cable
6	HDD TRANSFER BOARD 370P	55.48403.001	9811802-0001	43	w/ connector
7	KEYBOARD TRANSFER BOARD 370P	55.48404.001	9811803-0001		w/connector, mylar
8	CMOS BATTERY ASSY. (ASSY RTC BTY MODULE 370P)	60.48416.001	9811804-0001		BT1
9	(BIOS IC) IC MASKROM M38802M2-013HP 64P	85.45001.001	9811807-0001		U16
10	LOGO PLATE, EXT 610	40.46813.041	9811819-0001		
11	LOGO PLATE, EXT 610CD	40.46813.051	9811820-0001		
12	LOGO PLATE, EXT 610CDT	40.46813.061	9811821-0001		
13	LOGO PLATE, EXT 616	40.46813.101	9815703-0001		
14	CLOSE COVER SWITCH (W.A. 2P 50MM W/CVR SW,EXT 61X)	50.46911.021	9811822-0001		
15	KNOB TH (MOUSE BUTTONS)	42.46912.001	9811823-0001	23	
16	COVER, SIMM MEMORY,EXT 61X	34.46904.001	9815575-0001	87	
17	CABLE ASSY, TOUCHPAD-FPC,EXT 61X	50.48401.001	9815577-0001		
18	HDD DOOR, EXT 61X	42.46905.002	9815578-0001		
19	EXT FDD COVER (RUBBER DOOR), EXT 61X	47.46903.001	9815580-0001	67	
20	I/O DOOR (REAR), EXT 61X	6M.48416.001	9815581-0001	78, 79	w/latch
21	SPEAKER 0.3W T023S03	23.40015.021	9815596-0001	41	
22	BATTERY BOARD	55.46904.001	9815597-0001		w/ assy. cable
23	ASSY FDD INTERNAL	91.46905.011	9811787-0001	62	w/ bracket, cable, bezel, knob, lens
24	FDD 1.44 3.5" D353F2 MIT	see above kit	see above kit		
25	ASSY FDD BZL	see above kit	see above kit	67	with bezel & lens
26	FDD CABLE	50.46902.001	9815426-0001	63	
27	BATTERY DOOR	42.46955.001	9815598-0001	29	

Table C1 Spare parts list (continued)

	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
KEYBOARDS					
	KB-84 KEY KAS1901-0161R US 370 (US)	90.46907.001	9805728-0001	27	w/cable
	Keyboard(UK)	90.46907.00U	9805758-0002	27	w/cable
	Keyboard(Germany)	90.46907.00G	9805758-0003	27	w/cable
	Keyboard(French)	90.46907.00F	9805758-0004	27	w/cable
	Keyboard(Spanish)	90.46907.00S	9805758-0005	27	w/cable
	Keyboard(Sws/Ger)	90.46907.007	9805758-0006	27	w/cable
	Keyboard(Italian)	90.46907.00I	9805758-0007	27	w/cable
	Keyboard(Portuguese)	90.46907.00P	9805758-0008	27	w/cable
	Keyboard(Sweden)	90.46907.00W	9805758-0010	27	w/cable
	Keyboard(Denmark)	90.46907.00D	9805758-0012	27	w/cable
	Keyboard(Norwegian)	90.46907.00N	9805758-0013	27	w/cable
	Keyboard(Finland)	90.46907.008	9805758-0014	27	w/cable
	Keyboard(Belgium)	90.46907.00B	9805758-0015	27	w/cable
	Keyboard(Chinese)	90.46907.00C	9805758-0019	27	w/cable
	Keyboard(Korean)	90.46907.00K	9805758-0020	27	w/cable
	Keyboard(Japanese)	90.46907.00J	9805758-0021	27	w/cable

Table C1 Spare parts list (continued)

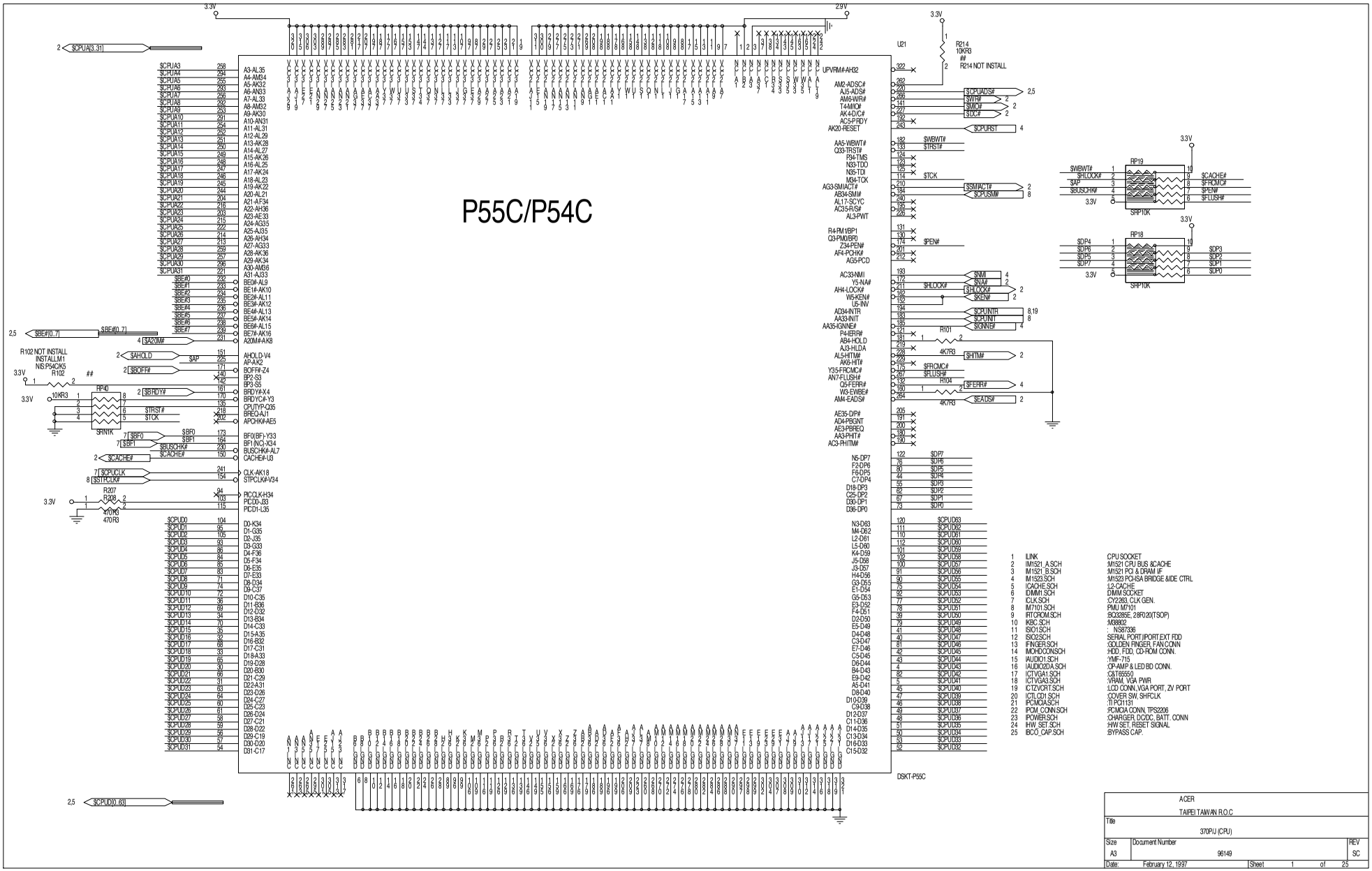
	PART NAME	ACER P/N	TI P/N	Ref. Exploded View	COMMENTS
SERVICE KITS					
	MISC. PARTS PACK	6M.48409.001	9815599-0001		
1	SCREW LCD CAP(47.46901.001) * 10 PCS		see above kit		
2	CAP RUBBER(47.46917.001) * 10 PCS		see above kit		
3	CLIPPER CABLE(42.46921.001) * 10 PCS		see above kit		
4	RUBBER FOOT (47.46902.001) * 10 PCS		see above kit		
5	FOOT PU BLACK (47.45001.001)*10 PCS		see above kit		
6	CD LATCH(42.46903.001) * 10 PCS		see above kit		
	SCREW PACK	6M.48419.001	9815700-0001		
1	M2L4(86.1A352.4R0) * 10 PCS		see above kit		
2	M2L5(86.1AL22.5R0) * 10 PCS		see above kit		
3	M2L14(86.1A522.140) * 10 PCS		see above kit		
4	M2.5L5(86.4A553.5R0) * 10 PCS		see above kit		
5	M2.5L6(BLACK)(86.1AI23.6R0) * 10 PCS		see above kit		
6	M2.5L6(86.1A553.6R0) * 10 PCS		see above kit		
7	M2.5L8(86.1A553.8R0) * 10 PCS		see above kit		
8	M2.5L18(86.1A523.180) * 10 PCS		see above kit		
9	M3L6 (86.4A524.6R0) * 10 PCS		see above kit		
	MYLAR PACK	6M.48420.001	9815701-0001		
1	MYLAR TH(40.46911.001)		see above kit		
2	MYLAR HDD BELT(40.48401.061)		see above kit	102	
	PCMCIA DOOR PACK	6M.48421.001	9815702-0001	69,34,35,36	
1	PCMCIA DOOR SPRING UPPER(34.46903.001) * 10 PCS		see above kit		
2	PCMCIA DOOR SPRING LOWER(34.46928.001) * 10 PCS		see above kit		
3	PCMCIA DOOR UPPER (42.46913.001) * 5 PCS		see above kit		
4	PCMCIA DOOR LOWER(42.46919.001) * 5 PCS		see above kit		

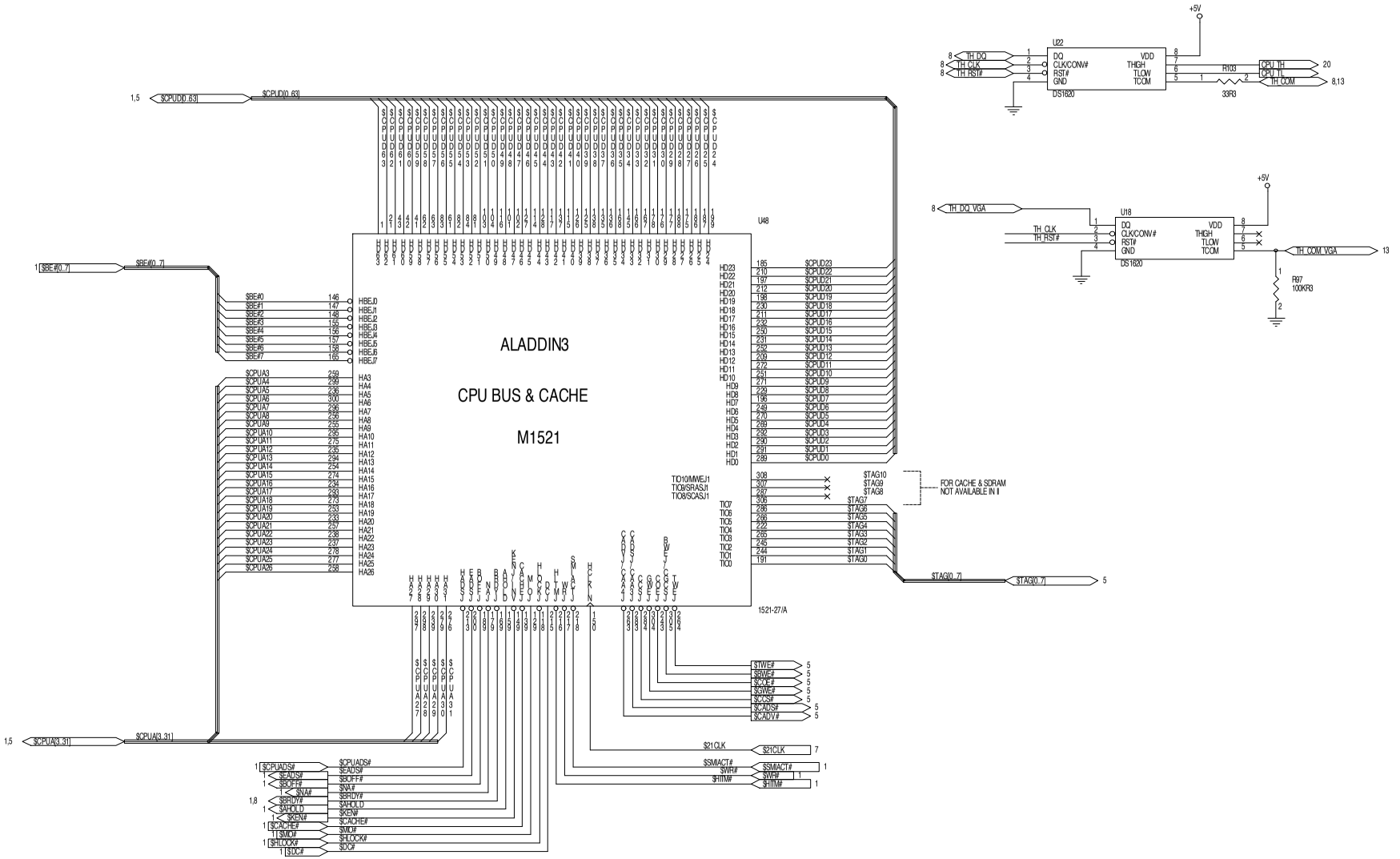
Table C1 Spare parts list (continued)

	PART NAME	ACER P/N	TI P/N
options			
	Misc.		
	EXT BTY CHARGER 91.48428.001 370P ONLY	91.48428.001	9811764-0001
	EXT FLOPPY DRIVE 91.46905.002 370/370P	91.46905.002	9811765-0001
	PS/2 CABLE 50.46812.001	50.46812.001	9811766-0001
	FILE TRANSFER CABLE 50.30014.001	50.30014.001	9811767-0001
	Power		
	AC ADAPTER ASSY,EXTENSA 61X w/power cord	91.48428.011	9811754-0001
	BATTERY PACK,EXTENSA 61X,NIMH SANYO	91.46928.012	9811738-0001
	BATTERY PACK,EXTENSA 61X,NIMH TOSHIBA	91.46928.007	9811738-0003
	LI-ION 91.46928.003 370/370P, EXT61X	91.46928.003	9811763-0001
	Memory		
	8 MB memory modules	91.46910.001	9811344-0001
	16 MB memory modules	91.46910.002	9811344-0002
	32 MB memory modules	91.46910.003	9811344-0003

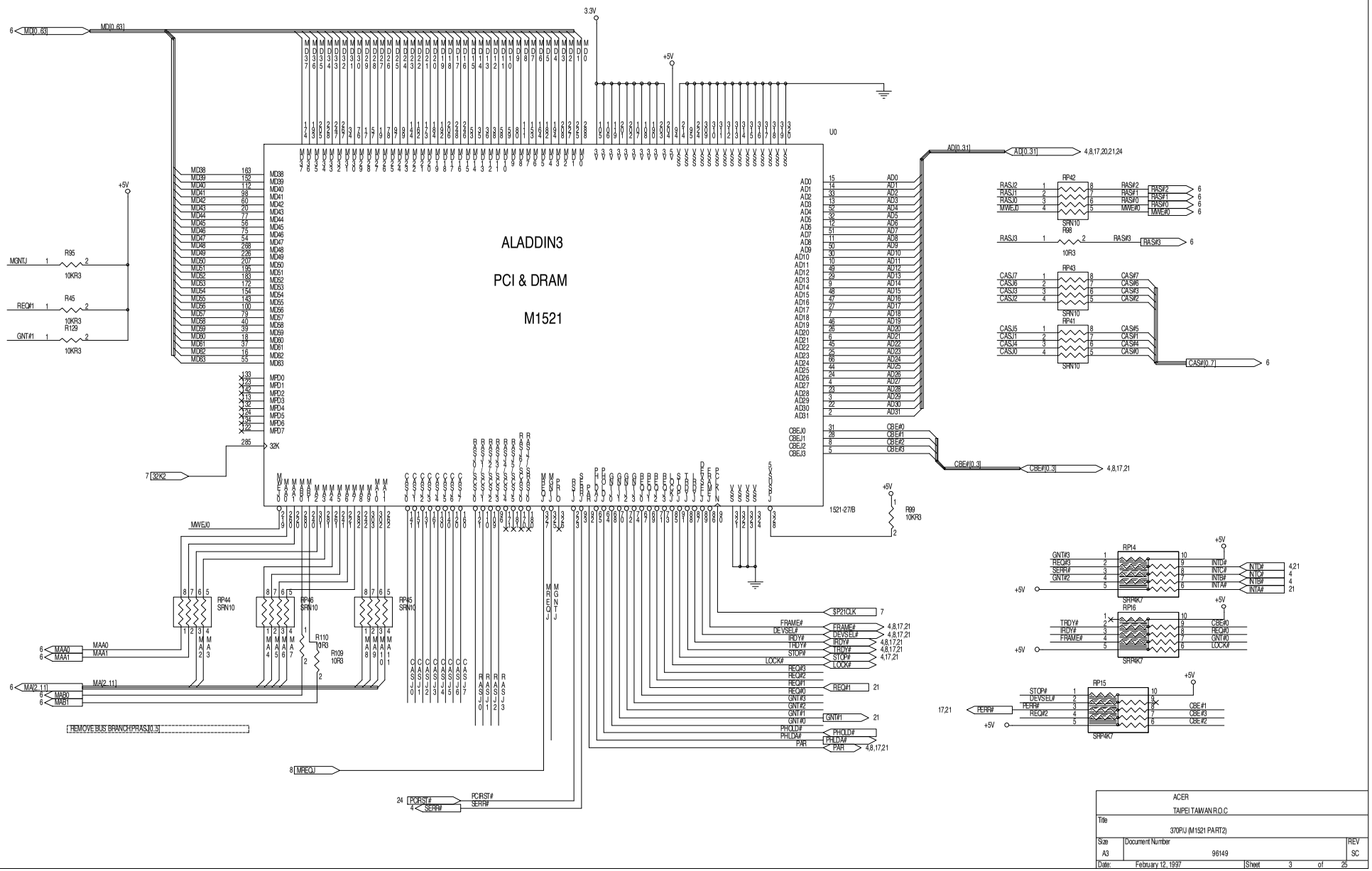
Schematics

This appendix shows the schematic diagrams of the notebook.


P55C/P54C
DSKT-P55C
U21
RP19
RP18
RP40
SHP10K
SHRN1K
R214 10KR3 ## R214 NOT INSTALL
R102 NOT INSTALL INSTALLM1 N/S:P54CK5
R207 470R3
R208 470R3
R101 4K7R3
R104 4K7R3
2 $CPUA[3..31]
2.5 $BE#[0..7]
2.5 $CPUD[0..63]
3.3V
2.9V
$CPUA3 258 A3-AL35
$CPUA4 254 A4-AM34
$CPUA5 255 A5-AK32
$CPUA6 253 A6-AN33
$CPUA7 256 A7-AL33
$CPUA8 252 A8-AM32
$CPUA9 253 A9-AK30
$CPUA10 251 A10-AN31
$CPUA11 254 A11-AL31
$CPUA12 252 A12-AL29
$CPUA13 251 A13-AK28
$CPUA14 250 A14-AL27
$CPUA15 249 A15-AK26
$CPUA16 248 A16-AL25
$CPUA17 247 A17-AK24
$CPUA18 246 A18-AL23
$CPUA19 245 A19-AK22
$CPUA20 244 A20-AL21
$CPUA21 204 A21-AF34
$CPUA22 216 A22-AH36
$CPUA23 203 A23-AE33
$CPUA24 215 A24-AG35
$CPUA25 222 A25-AJ35
$CPUA26 214 A26-AH34
$CPUA27 213 A27-AG33
$CPUA28 209 A28-AK36
$CPUA29 257 A29-AK34
$CPUA30 206 A30-AM36
$CPUA31 221 A31-AJ33
$BE#0 232 BE0#-AL9
$BE#1 233 BE1#-AK10
$BE#2 234 BE2#-AL11
$BE#3 235 BE3#-AK12
$BE#4 236 BE4#-AL13
$BE#5 237 BE5#-AK14
$BE#6 238 BE6#-AL15
$BE#7 239 BE7#-AK16
4 $A20M# 231 A20M#-AK8
2 $AHOLD 151 AHOLD-V4
$AP 225 AP-AK2
2 $BOFF# 171 BOFF#-Z4
140 BP2-S3
142 BP3-S5
2 $BRDY# 161 BRDY#-X4
170 BRDYC#-Y3
135 CPUTYP-Q35
$TRST# 218 BREQ-AJ1
$TCK 202 APCHK#-AE5
$BF0 173 BF0(BF)-Y33
$BF1 164 BF1 (NC)-X34
$BUSCHK# 230 BUSCHK#-AL7
$CACHE# 150 CACHE#-U3
$CPUCLK 241 CLK-AK18
$STPCLK# 154 STPCLK#-V34
94 PICCLK-H34
103 PICD0-J33
115 PICD1-L35
$CPUD0 104 D0-K34
$CPUD1 95 D1-G35
$CPUD2 105 D2-J35
$CPUD3 93 D3-G33
$CPUD4 86 D4-F36
$CPUD5 84 D5-F34
$CPUD6 85 D6-E35
$CPUD7 83 D7-E33
$CPUD8 71 D8-D34
$CPUD9 74 D9-C37
$CPUD10 72 D10-C35
$CPUD11 36 D11-B36
$CPUD12 69 D12-D32
$CPUD13 34 D13-B34
$CPUD14 70 D14-C33
$CPUD15 35 D15-A35
$CPUD16 32 D16-B32
$CPUD17 68 D17-C31
$CPUD18 33 D18-A33
$CPUD19 65 D19-D28
$CPUD20 30 D20-B30
$CPUD21 66 D21-C29
$CPUD22 31 D22-A31
$CPUD23 63 D23-D26
$CPUD24 64 D24-C27
$CPUD25 60 D25-C23
$CPUD26 61 D26-D24
$CPUD27 58 D27-C21
$CPUD28 59 D28-D22
$CPUD29 56 D29-C19
$CPUD30 57 D30-D20
$CPUD31 54 D31-C17
UPVRM#-AH32
AM2-ADSC#
AJ5-ADS#
AM6-WR#
T4-MIO#
AK4-D/C#
AC5-PHDY
AK20-RESET
AA5-WBWT#
Q33-TRST#
P34-TMS
N33-TDO
N35-TDI
M34-TCK
AG3-SMIACT#
AB34-SMI#
AL17-SCYC
AC35-HLS#
AL3-PWT
R4-PM1BP1
Q3-PM0BP0
Z34-PEN#
AF4-PCHK#
AG5-PCD
AC33-NMI
Y5-NA#
AH4-LOCK#
W5-KEN#
U5-INV
AD34-INTR
AA33-INIT
AA35-IGNNE#
P4-IERR#
AB4-HOLD
AJ3-HLDA
AL5-HITM#
AK6-HIT#
Y35-FRCMC#
AN7-FLUSH#
Q5-FERR#
W3-EWBE#
AM4-EADS#
AE35-DP#
AD4-PBGNT
AE3-PBREQ
AA3-PHIT#
AC3-PHITM#
N5-DP7
F2-DP6
F6-DP5
C7-DP4
D18-DP3
C25-DP2
D30-DP1
D36-DP0
N3-D63
M4-D62
L2-D61
L5-D60
K4-D59
J5-D58
J3-D57
H4-D56
G3-D55
E1-D54
G5-D53
E3-D52
F4-D51
D2-D50
E5-D49
D4-D48
C3-D47
E7-D46
C5-D45
D6-D44
B4-D43
E9-D42
A5-D41
D8-D40
D10-D39
C9-D38
D12-D37
C11-D36
D14-D35
C13-D34
D16-D33
C15-D32
$SMIACT# 2
$SMI# 4
$NA# 2
$SHLOCK# 2
$KEN# 2
$INTR 8,19
$INIT 8
$IGNNE# 4
$HITM# 2
$FRCMC#
$FLUSH#
$FERR# 4
$EADS# 2
$SMI#
$NA#
$SHLOCK#
$KEN#
$INTR
$INIT
$IGNNE#
$HITM#
$FRCMC#
$FLUSH#
$FERR#
$EADS#
$CPUADS# 2,5
$WR# 2
$MIO# 2
$D/C# 2
$CPURST 4
$WBWT#
$TRST#
$TCK
$SMIACT#
$CPUSMI# 8
$PEN#
$WBWT#
$SHLOCK#
$AP
$BUSCHK#
$CACHE#
$PEN#
$FLUSH#
$SDP4
$SDP6
$SDP5
$SDP7
$SDP3
$SDP2
$SDP1
$SDP0
$SD#7
$SD#6
$SD#5
$SD#4
$SD#3
$SD#2
$SD#1
$SD#0
$CPUD63
$CPUD62
$CPUD61
$CPUD60
$CPUD59
$CPUD58
$CPUD57
$CPUD56
$CPUD55
$CPUD54
$CPUD53
$CPUD52
$CPUD51
$CPUD50
$CPUD49
$CPUD48
$CPUD47
$CPUD46
$CPUD45
$CPUD44
$CPUD43
$CPUD42
$CPUD41
$CPUD40
$CPUD39
$CPUD38
$CPUD37
$CPUD36
$CPUD35
$CPUD34
$CPUD33
$CPUD32
1 ILINK ;CPU SOCKET
2 IM1521_A.SCH ;M1521 CPU BUS &CACHE
3 IM1521_B.SCH ;M1521 PCI & DRAM IF
4 IM1523.SCH ;M1523 PCHSA BRIDGE &IDE CTRL
5 ICACHE.SCH ;L2-CACHE
6 IDIMM1.SCH ;DIMM SOCKET
7 ICLK.SCH ;CY2263, CLK GEN.
8 IM7101.SCH ;PMU M7101
9 IRTCROM.SCH ;BQ3285E, 28F020(TSOP)
10 IKBC.SCH ;M38802
11 ISIO1.SCH ; N387936
12 ISIO2.SCH ;SERIAL PORT,IPORT,EXT FDD
13 IFINGER.SCH ;GOLDEN FINGER, FAN CONN
14 IMOHDCONSCH ;HDD, FDD, CD-ROM CONN.
15 IAUDIO1.SCH ;YMF-715
16 IAUDIO2.A.SCH ;OP-AMP & LED BD CONN.
17 ICTVGA1.SCH ;C&T65550
18 ICTVGA3.SCH ;VRAM, VGA PWR
19 ICTZVORT.SCH ;LCD CONN, VGA PORT, ZV PORT
20 ICTLCD1.SCH ;COVER SW, SHFCLK
21 IPCMCIA.SCH ;TI PCI1131
22 IPCM_CONN.SCH ;PCMCIA CONN, TPS2206
23 IPOWER.SCH ;CHARGER, D/CDC, BATT. CONN
24 IHW_SET.SCH ;H/W SET, RESET SIGNAL
25 IBCO_CAP.SCH ;BYPASS CAP.
ACER
TAIPEI TAIWAN R.O.C
Title
370P/J (CPU)
Size A3
Document Number 96149
REV SC
Date: February 12, 1997
Sheet 1 of 25



ACER			
TAIPEI TAIWAN R.O.C			
Title: 370RU (M1521 CPU TO PCI BRIDGE)			
Size: A3	Document Number: 96149		REV: SC
Date: February 12, 1997	Sheet 2 of 25		


ALADDIN3
PCI & DRAM
M1521
U0
1521-27/B
MD[0..63]
AD[0..31]
CBE#[0..3]
MAA0
MAA1
MA[2..11]
MAB0
MAB1
MWEJ0
MREQJ
MGNTJ
REQ#1
GNT#1
R95
10KR3
R45
10KR3
R129
10KR3
R99
10KR3
R110
10R3
R109
10R3
R98
10R3
RP42
SRN10
RP43
SRN10
RP41
SRN10
RP44
SRN10
RP46
SRN10
RP45
SRN10
RP14
SHP4K7
RP16
SHP4K7
RP15
SHP4K7
RASJ2
RASJ1
RASJ0
MWEJ0
RASJ3
CASJ7
CASJ6
CASJ3
CASJ2
CASJ5
CASJ1
CASJ4
CASJ0
RASJ[0..3]
CASJ[0..7]
$P21CLK
FRAME#
DEVSEL#
IRDY#
TRDY#
STOP#
LOCK#
REQJ3
REQJ2
REQJ1
REQJ0
GNTJ3
GNTJ2
GNTJ1
GNTJ0
PHOLD#
PHLDA#
PAR
GNT#1
REQ#1
PCIRST#
SERR#
PERR#
REQ#2
GNT#3
REQ#3
SERR#
GNT#2
INTD#
INTC#
INTB#
INTA#
TRDY#
IRDY#
FRAME#
STOP#
DEVSEL#
PERR#
REQ#2
CBE#1
CBE#3
CBE#2
REMOVE BUS BRANCH PRASJ[0..5]
3.3V
+5V
ACER
TAIPEI TAIWAN R.O.C
Title
370PIJ (M1521 PART2)
Size
A3
Document Number
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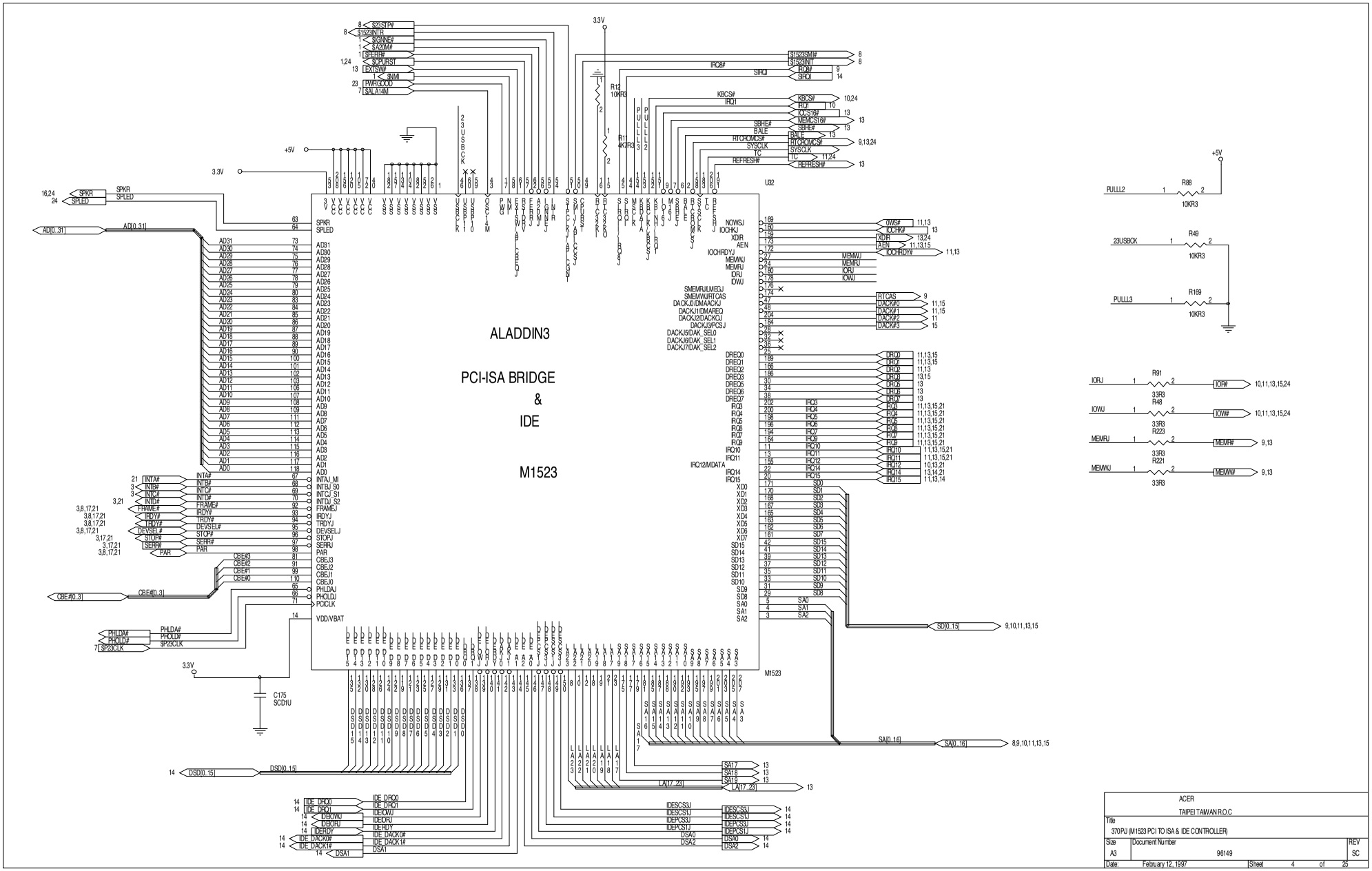
ALADDIN3
PCI-ISA BRIDGE
&
IDE
M1523
U82
M1523
3.3V
+5V
R12
10KR3
R11
4K7R3
C175
SCD1U
R88
10KR3
R49
10KR3
R169
10KR3
R91
33R3
R48
33R3
R223
33R3
R221
33R3
ACER
TAIPEI TAIWAN R.O.C
Title
370PU (M1523 PCI TO ISA & IDE CONTROLLER)
Size
A3
Document Number
96149
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Date:
February 12, 1997
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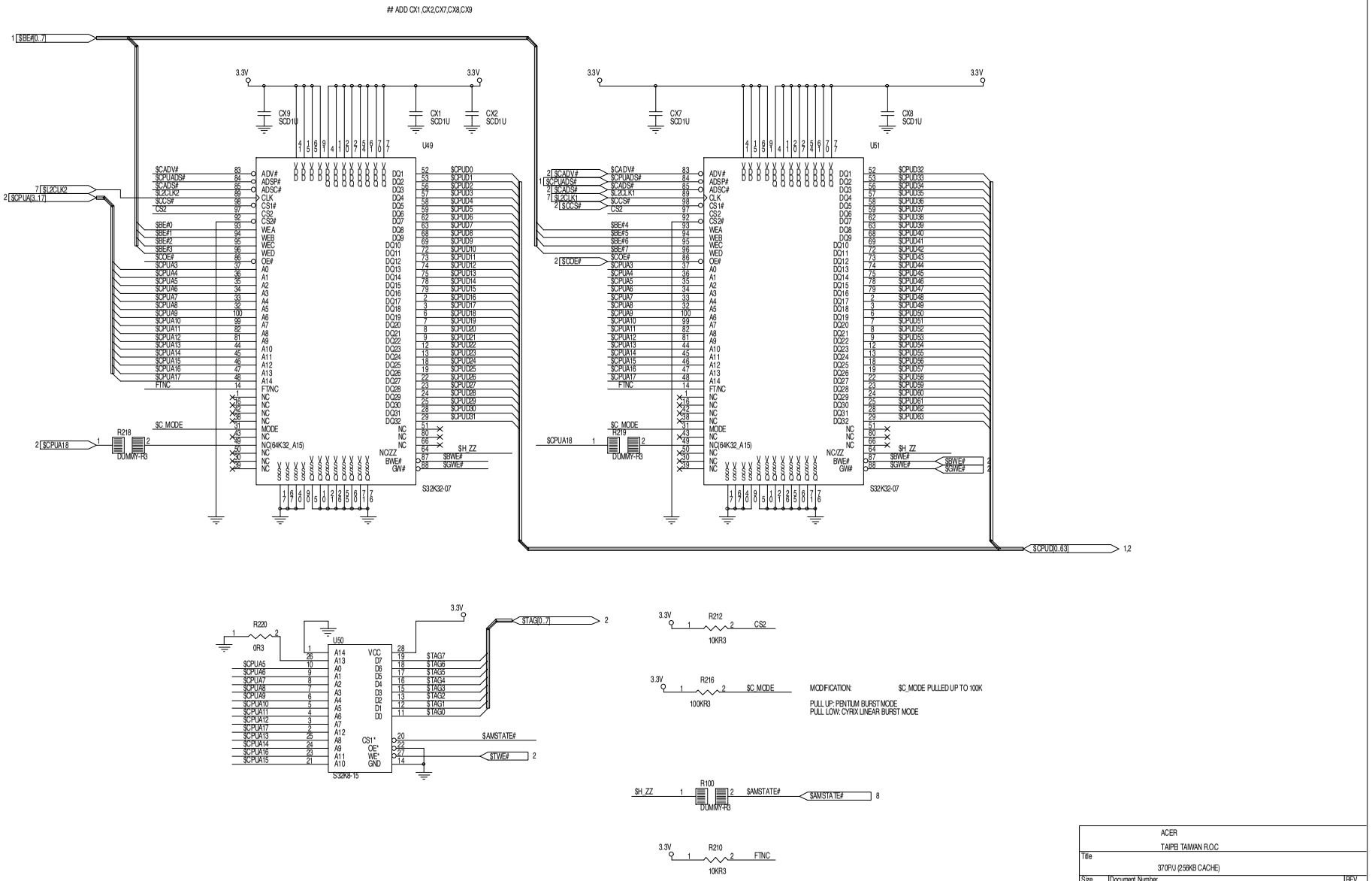
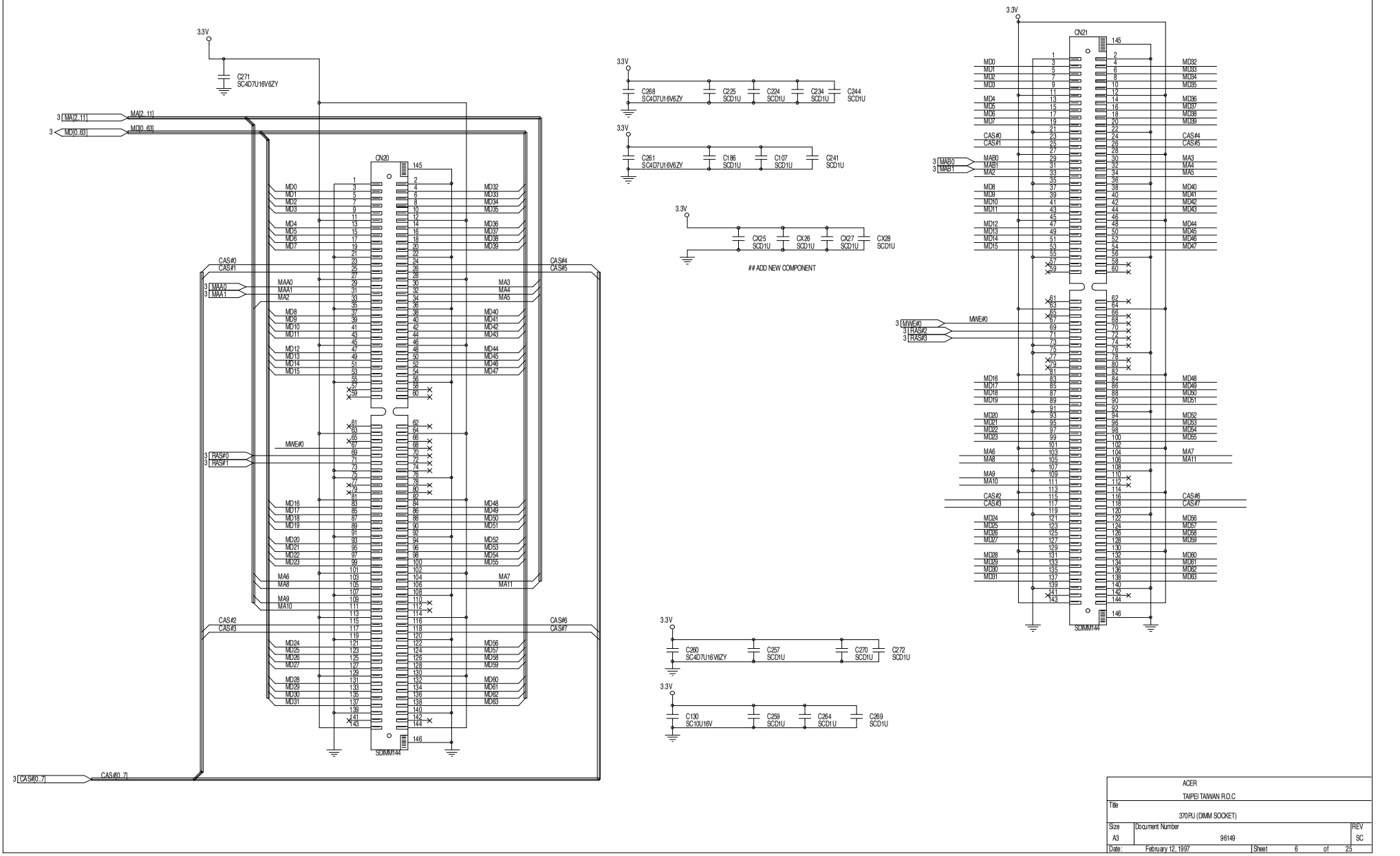


ACER		
TAIPEI TAIWAN R.O.C		
Title	370P/J (256KB CACHE)	
Size: A3	Document Number: 96149	REV: SC
Date: February 12, 1997	Sheet 5 of 25	



ACER			
TAIPEI TAIWAN R.O.C			
Title	370PJ (DIMM SOCKET)		
Size	Document Number		REV
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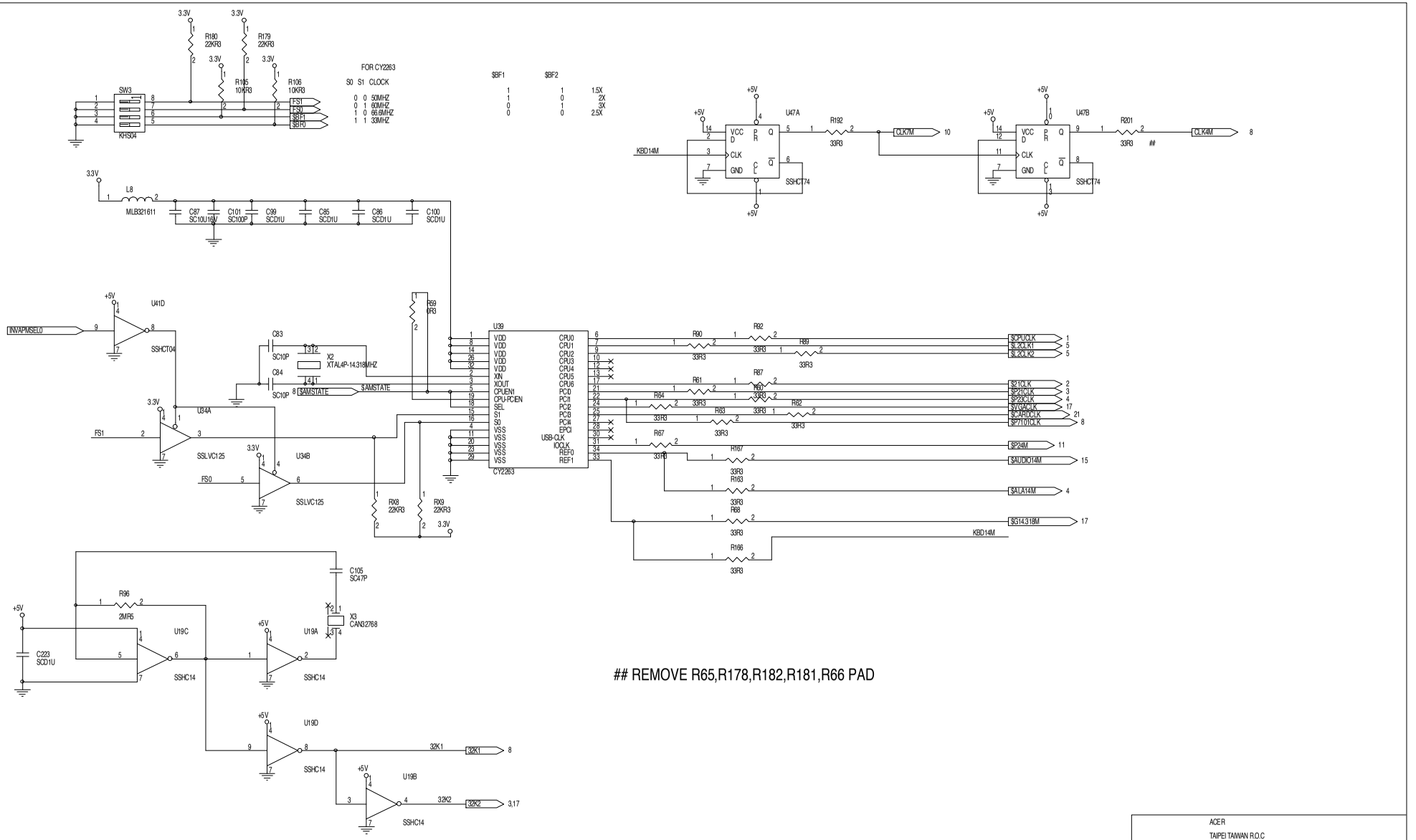
Date:	February 12, 1997	Sheet 6 of 25	


FOR CY2263
S0 S1 CLOCK
0 0 50MHZ
0 1 60MHZ
1 0 66.6MHZ
1 1 33MHZ
$BF1 $BF2
1 1 1.5X
1 0 2X
0 1 3X
0 0 2.5X
SW3
KHS04
R180 22KR3
R179 22KR3
R105 10KR3
R106 10KR3
FS1
FS0
SBF1
SBF0
L8
MLB321611
C87 SC10U16V
C101 SC100P
C99 SCD1U
C85 SCD1U
C86 SCD1U
C100 SCD1U
U41D
SSHCT04
INVAPMSEL0
C83 SC10P
C84 SC10P
X2 XTAL4P-14.318MHZ
SAMSTATE
R69 0R3
U39
CY2263
VDD
VSS
XIN
XOUT
CPUEN1
CPU-PCIEN
SEL
S1
S0
CPU0
CPU1
CPU2
CPU3
CPU4
CPU5
CPU6
PCI0
PCI1
PCI2
PCI3
PCI4
PCI5
USB-CLK
IOCLK
REF0
REF1
R90 33R3
R92 33R3
R89 33R3
R87 33R3
R61 33R3
R64 33R3
R63 33R3
R62 33R3
R67 33R3
R167 33R3
R163 33R3
R68 33R3
R166 33R3
3CPUCLK
3L2CLK1
3L2CLK2
3T1CLK
3P21CLK
3P22CLK
3V10CLK
3CARDCLK
3P710CLK
3P24M
3AUDIO14M
3ALAT14M
3G14.318M
KBD14M
U34A
U34B
SSLVC125
RX8 22KR3
RX9 22KR3
U47A
U47B
SSHCT74
R192 33R3
R201 33R3
CLK7M
CLK4M
C105 SC47P
X3 CAN32768
R96 2MR5
C223 SCD1U
U19C
U19A
U19D
U19B
SSHC14
32K1
32K2
REMOVE R65,R178,R182,R181,R66 PAD
ACER
TAIPEI TAIWAN R.O.C
Title
370P/J (CY2263 CLOCK GENERATOR)
Size A3
Document Number 96149
REV SC
Date: February 12, 1997
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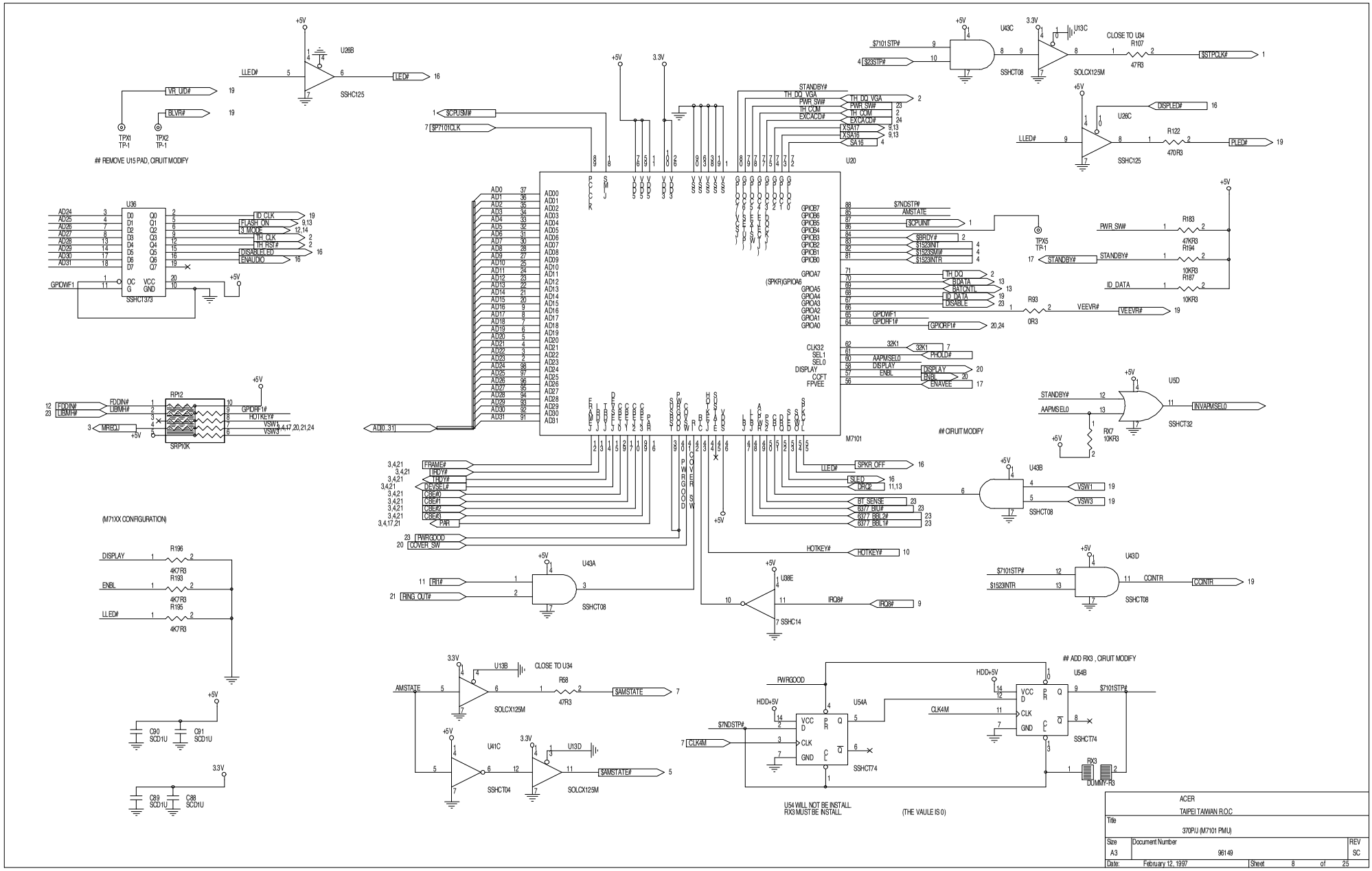
U26B
SSHC125
LLED#
LED#
VR_UID#
BLVH#
TPX1 TP-1
TPX2 TP-1
REMOVE U15 PAD, CIRUIT MODIFY
U43C
SSHC08
$7101STP#
$23STP#
U13C
SOLCX125M
CLOSE TO U34
R107
47R3
$STPCLK#
U26C
SSHC125
DISPLED#
PLED#
R122
470R3
U20
STANDBY#
TH_DQ_VGA
PWR_SW#
TH_COM
EXCACD#
XSA17
XSA16
SA16
SCPUSMI#
$P7101CLK
U36
SSHC1373
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
ID_CLK
FLASH_ON
3_MODE
TH_CLK
TH_RST#
DISABLELED
ENAUDIO
GPIOWF1
M7101
AD[0..31]
$7NDSTP#
AMSTATE
$CPUINIT
$SRDY#
$1523INT
$1523SMI#
$1523INTR
GPIOA7
(SPKR)GPIOA6
GPIOA5
GPIOA4
GPIOA3
GPIOA2
GPIOA1
GPIOA0
GPIOWF1
GPIORF1#
CLK32
SEL1
SEL0
DISPLAY
CCFT
FPVEE
TH_DQ
BDATA
BAYCNTL
ID_DATA
DISABLE
32K1
PHOLD#
AAPMSEL0
DISPLAY
ENBL
ENAVEE
TPX5 TP-1
PWR_SW#
R183
47KR3
R194
STANDBY#
10KR3
R187
ID_DATA
10KR3
R93
0R3
VEEVR#
CIRUIT MODIFY
U5D
SSHCT32
INVAPMSEL0
RX7
10KR3
RIP12
SRP10K
FDDIN#
LIBMH#
MREQJ
GPIORF1#
HOTKEY#
VSW1
VSW3
20,21,24
FRAME#
IRDY#
TRDY#
DEVSEL#
CBE#0
CBE#1
CBE#2
CBE#3
PAR
PWRGOOD
COVER_SW
SPKR OFF
SLED
DRQ2
BT_SENSE
6377_BRUF
6377_BRL2#
6377_BRL1#
U43B
SSHCT08
VSW1
VSW3
HOTKEY#
U43A
RI#
RING_OUT#
U38E
SSHC14
IRQ8#
U43D
CCINTR
(M71XX CONFIGURATION)
R196
4K7R3
R193
4K7R3
R195
4K7R3
DISPLAY
ENBL
LLED#
C90 SCD1U
C91 SCD1U
C89 SCD1U
C88 SCD1U
U13B
SOLCX125M
CLOSE TO U34
R68
47R3
$AMSTATE
U41C
SSHCT04
U13D
$AMSTATE#
ADD RX3 , CIRUIT MODIFY
U54A
U54B
SSHCT74
HDD+5V
PWRGOOD
CLK4M
$7NDSTP#
$7101STP#
RX3
DUMMY-R3
U54 WILL NOT BE INSTALL.
RX3 MUST BE INSTALL.
(THE VAULE IS 0)
ACER
TAIPEI TAIWAN R.O.C
Title
370PU (M7101 PMU)
Size
A3
Document Number
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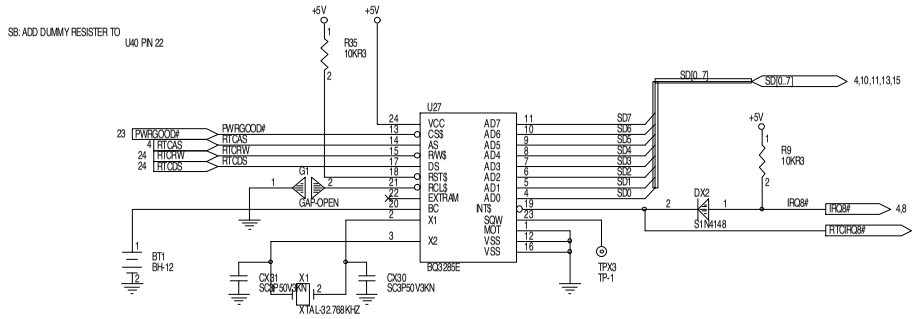
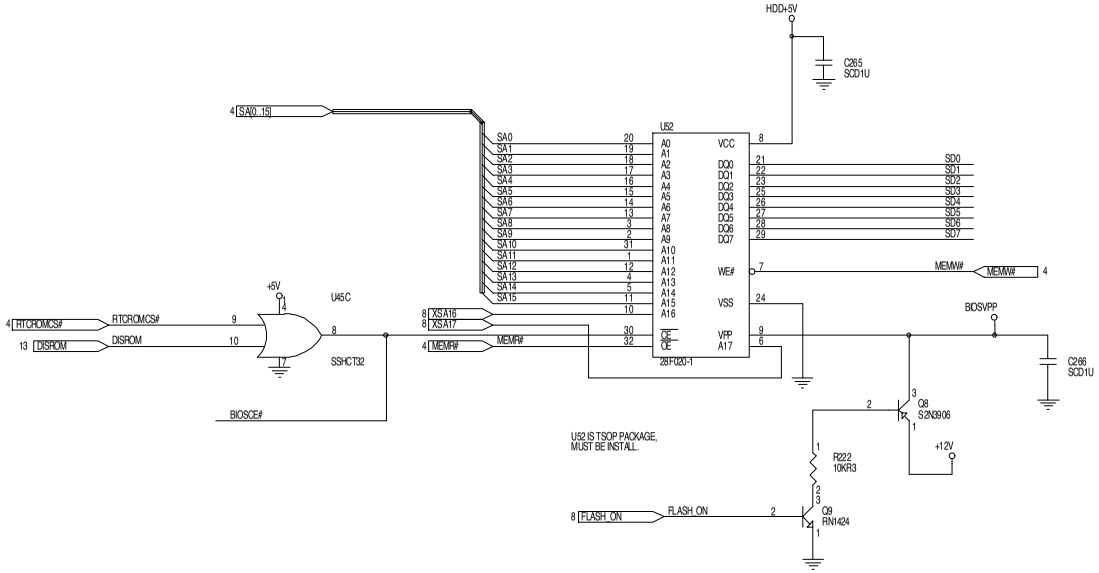
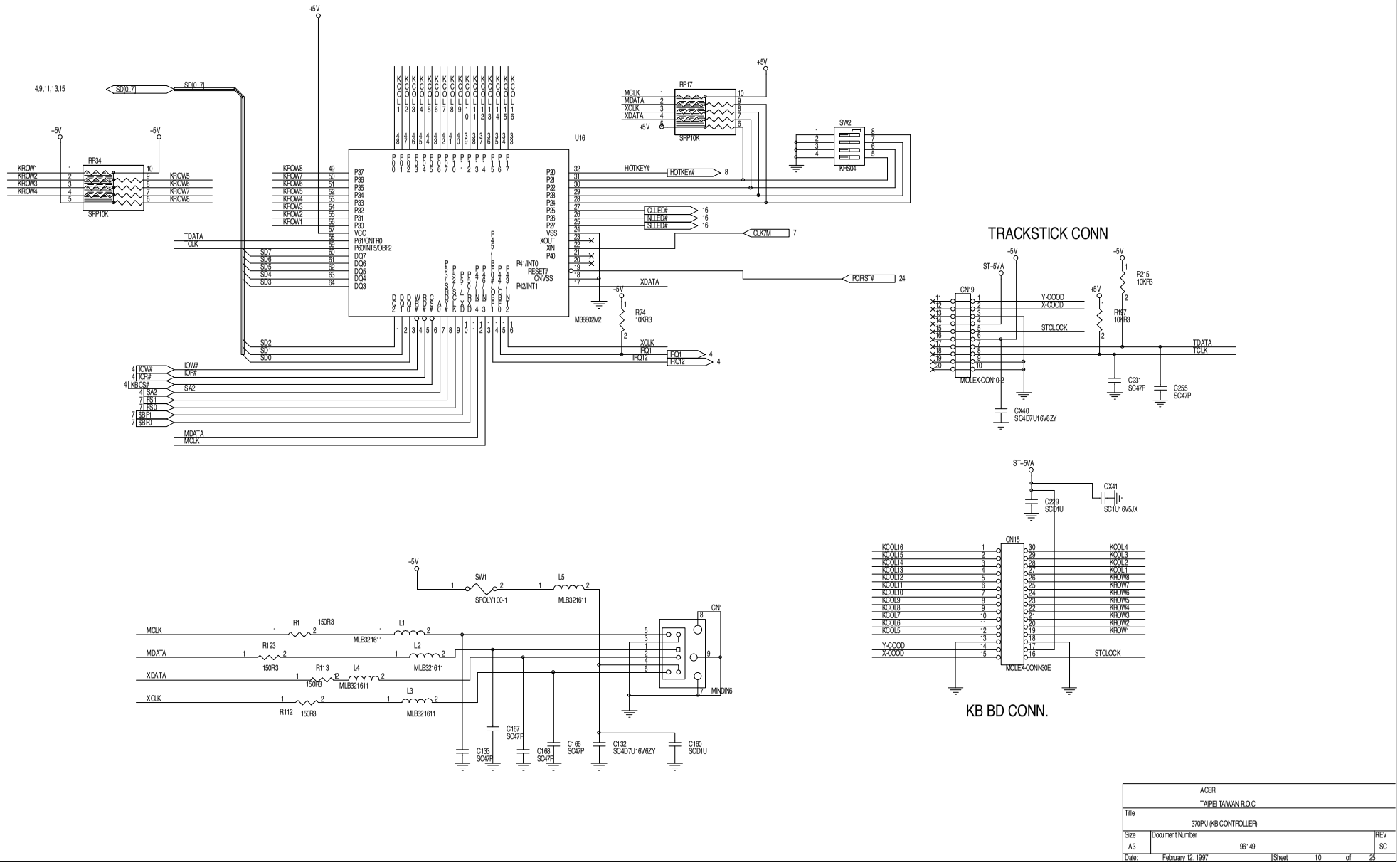


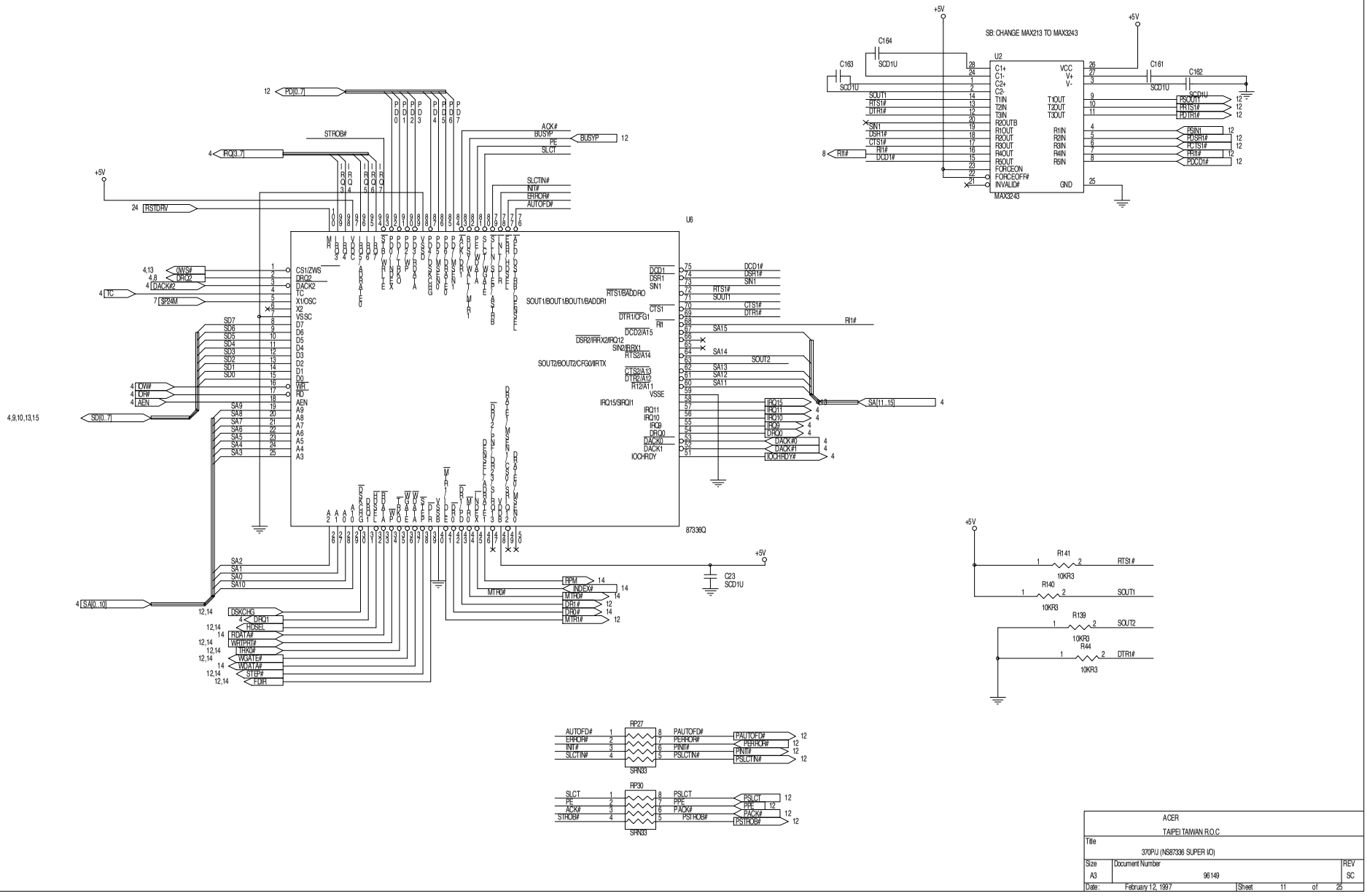


REMOVE U53 PAD

ACER			
TAIPEI TAIWAN R.O.C			
Title	370P/J (RTC AND BIOS)		
Size	Document Number		REV
A3	96149		SC
Date: February 12, 1997		Sheet 9 of 25	



ACER			
TAIPEI TAIWAN R.O.C			
Title	370PU (KB CONTROLLER)		
Size	Document Number		REV
A3	96149		SC
Date:	February 12, 1997	Sheet 10 of 25	


SB: CHANGE MAX213 TO MAX3243
U2
MAX3243
C164
C163
C161
C162
SCD1U
U6
87336Q
PD[0..7]
IRQ[3..7]
STROB#
ACK#
BUSY
PE
SLCT
SLCTIN#
INIT#
ERROR#
AUTOFD#
RSTDRV
SD[0..7]
SA[0..10]
SA[11..15]
IOW#
IOR#
AEN
DACK2
TC
SP24M
DRQ2
DRQ1
DRQ0
DACK0
DACK1
IOCHRDY
IRQ15
IRQ11
IRQ10
IRQ9
RTS1#
SOUT1
SOUT2
DTR1#
CTS1#
DSR1#
SIN1
RI1#
DCD1#
RPM
INDEX#
MTR0#
DS1#
DS0#
MTR1#
DSKCHG
HDSEL
RDATA#
WRTPRT#
TRK0#
WGATE#
WDATA#
STEP#
DIR
RP27
SHN83
RP30
PAUTOFD#
PERROR#
PINIT#
PSLCTIN#
PSLCT
PPE
PACK#
PSTROB#
R141
R140
R139
R44
10KR3
ACER
TAIPEI TAIWAN R.O.C
370PJ (NS87336 SUPER I/O)
Size
A3
Document Number
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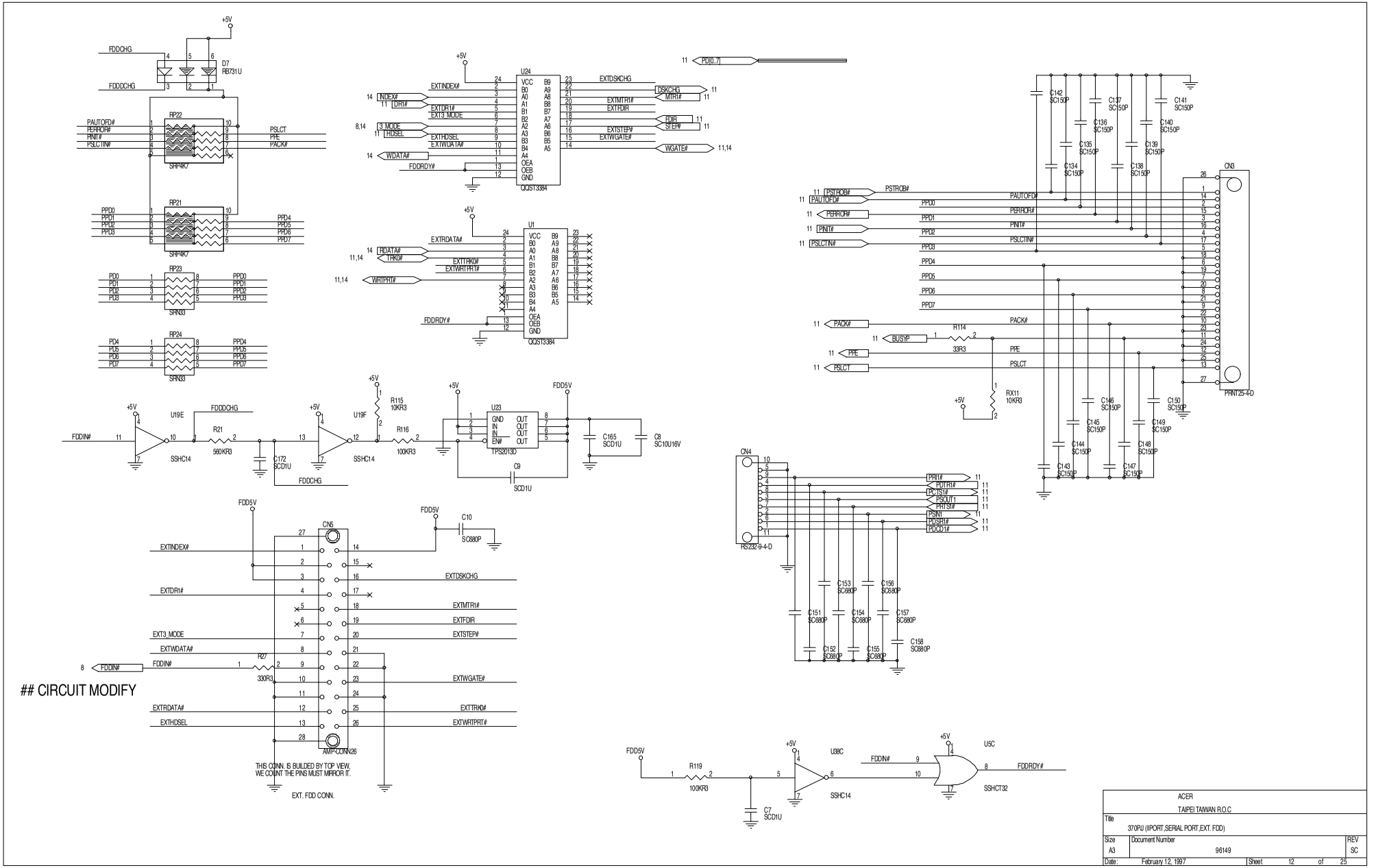
+5V
FDDCHG
D7
RB731U
RP22
SHP4K7
PAUTOFD#
PERROR#
PINIT#
PSLCTIN#
PSLCT
PPE
PACK#
RP21
PPD0
PPD1
PPD2
PPD3
PPD4
PPD5
PPD6
PPD7
RP23
SHN33
PD0
PD1
PD2
PD3
RP24
PD4
PD5
PD6
PD7
U24
QQST3384
EXTINDEX#
INDEX#
DIR#
EXTDIR1#
EXT3_MODE
3_MODE
HDSEL
EXTHDSEL
EXTWDATA#
WDATA#
FDDRDY#
EXTDSKCHG
DSKCHG
MTR1#
EXTMTR1#
EXTFDIR
FDIR
STEP#
EXTSTEP#
EXTWGATE#
WGATE#
11,14
PD0..7
U1
EXTRDATA#
RDATA#
THK0#
EXTTRK0#
EXTWRTPRT#
WRITPRT#
C142 SC150P
C137 SC150P
C141 SC150P
C136 SC150P
C140 SC150P
C135 SC150P
C139 SC150P
C134 SC150P
C138 SC150P
CN3
PRINT25-4-D
PSTROB#
R114
33R3
RX11
10KR3
C146 SC150P
C150 SC150P
C145 SC150P
C149 SC150P
C144 SC150P
C148 SC150P
C143 SC150P
C147 SC150P
U19E
SSHC14
FDDIN#
R21
560KR3
C172 SCD1U
U19F
R115 10KR3
R116
100KR3
U23
TPS2013D
GND
IN
EN#
OUT
C165 SCD1U
C8 SC10U16V
C9 SCD1U
CN4
RS232-9-4-D
PRT#
PDTR1#
PCTST#
PSOUT1
PRTST#
PSRT
PDSR1#
PDCD1#
C153 SC680P
C156 SC680P
C151 SC680P
C154 SC680P
C157 SC680P
C152 SC680P
C155 SC680P
C158 SC680P
CN5
AMP_CONN26
C10 SC680P
R27
330R3
EXTDSKCHG
EXTDR1#
EXTMTR1#
EXTFDIR
EXT3_MODE
EXTSTEP#
EXTWGATE#
EXTRDATA#
EXTTRK0#
EXTHDSEL
EXTWRTPRT#
THIS CONN. IS BUILDED BY TOP VIEW.
WE COUNT THE PINS MUST MIRROR IT.
EXT. FDD CONN.
R119
100KR3
C7 SCD1U
U8C
U5C
SSHCT32
FDDRDY#
CIRCUIT MODIFY
ACER
TAIPEI TAIWAN R.O.C
Title
370PJ (IPORT,SERIAL PORT,EXT. FDD)
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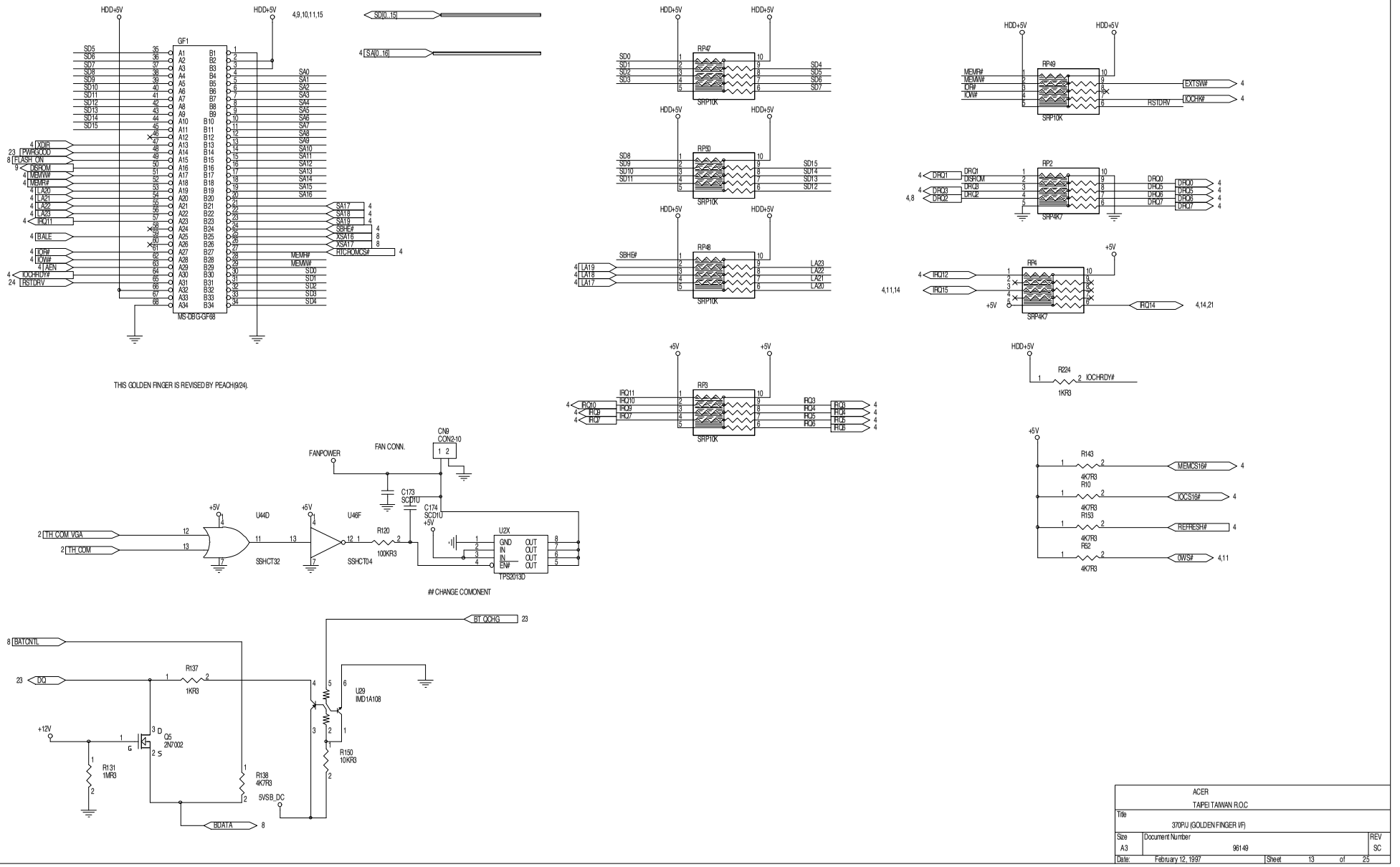

ACER			
TAIPEI TAIWAN R.O.C			
Title	370PU (GOLDEN FINGER I/F)		
Size	Document Number		REV
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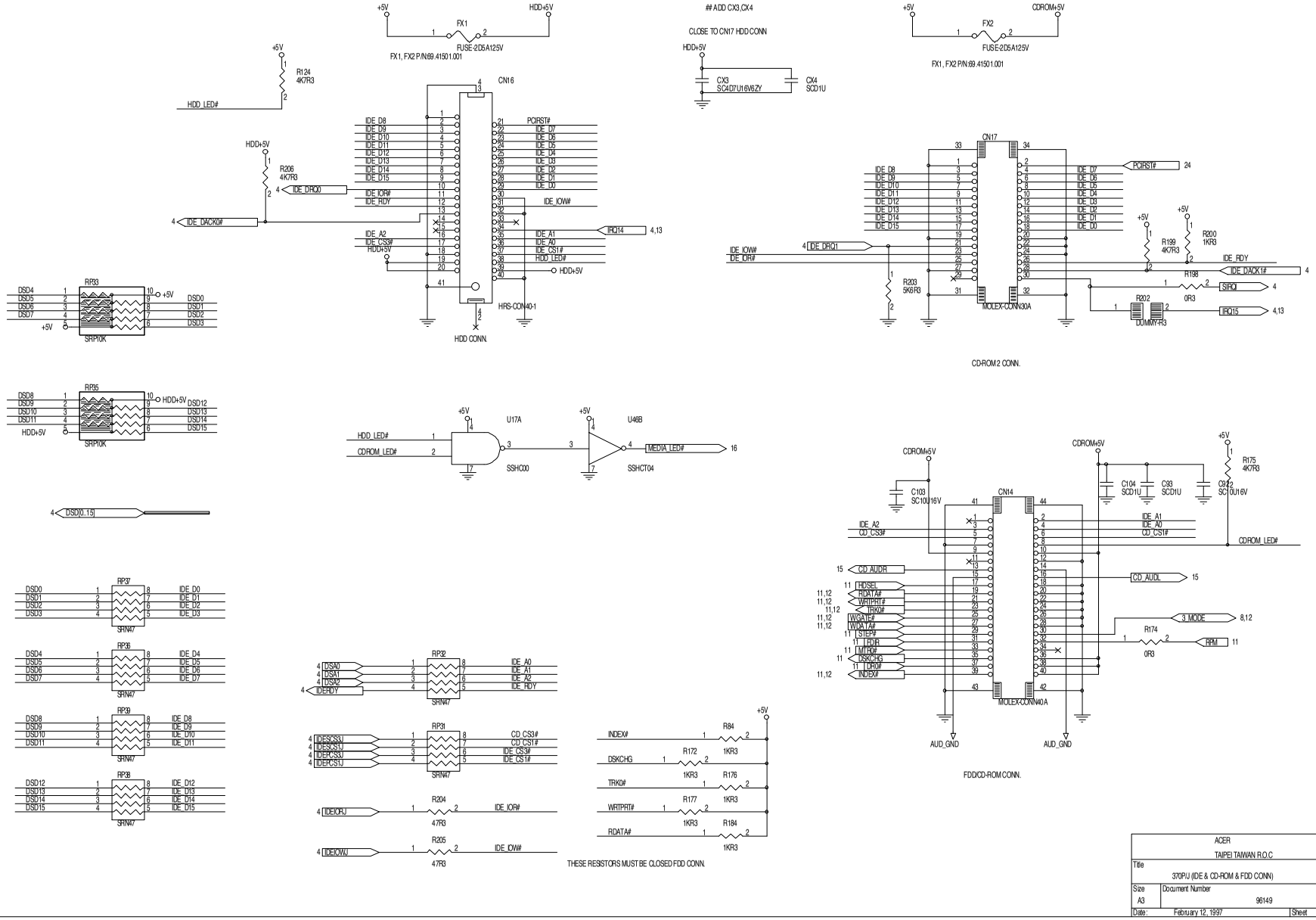

ACER			
TAIPEI TAIWAN R.O.C			
Title	370PJ (IDE & CD-ROM & FDD CONN)		
Size	Document Number		REV
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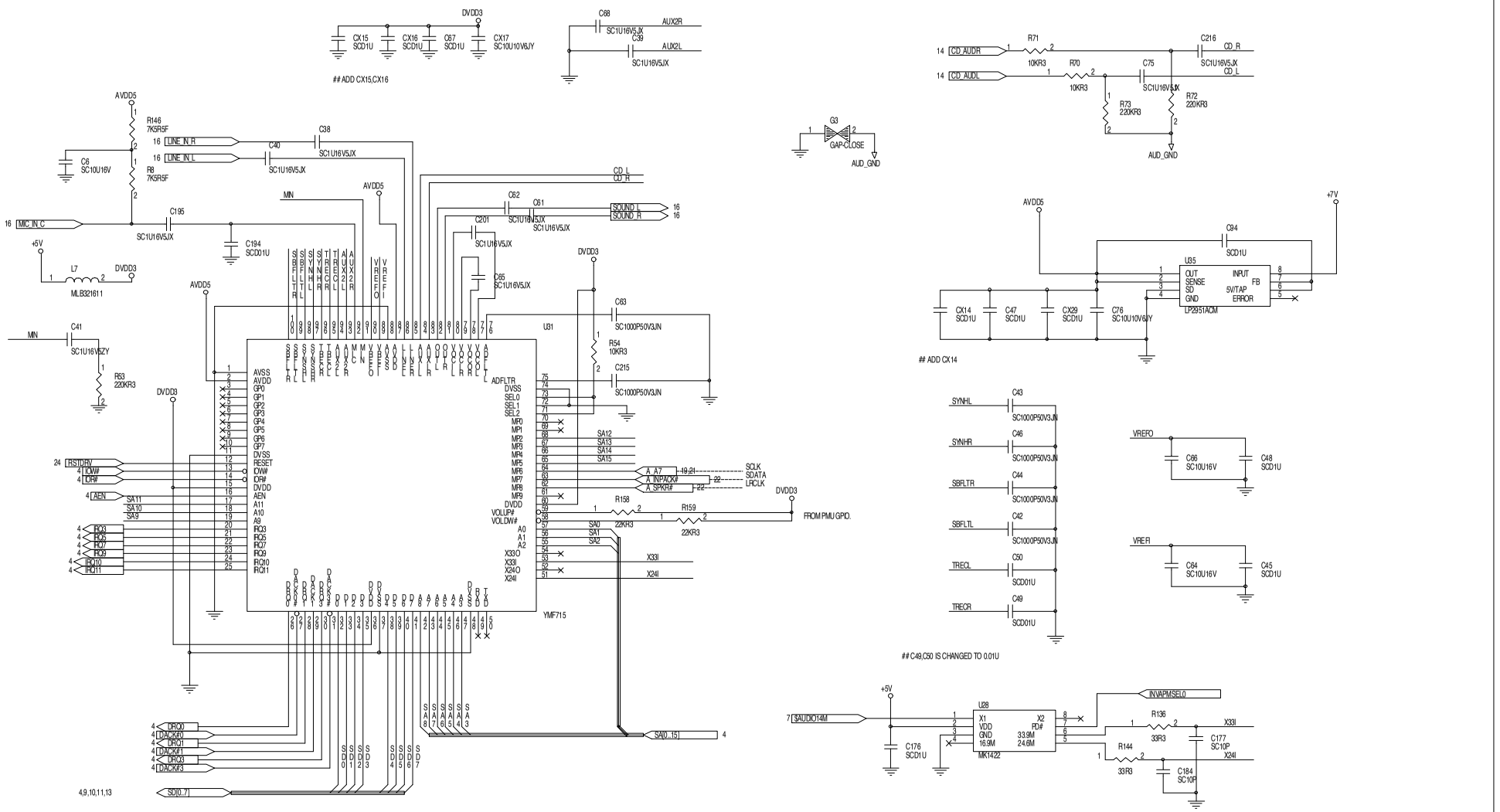
Date:	February 12, 1997	Sheet 14 of 25	



ACER		
TAIPEI TAIWAN R.O.C		
Title: 370PU (AUDIO YMF-715)		
Size: A3	Document Number: 96149	REV: SC
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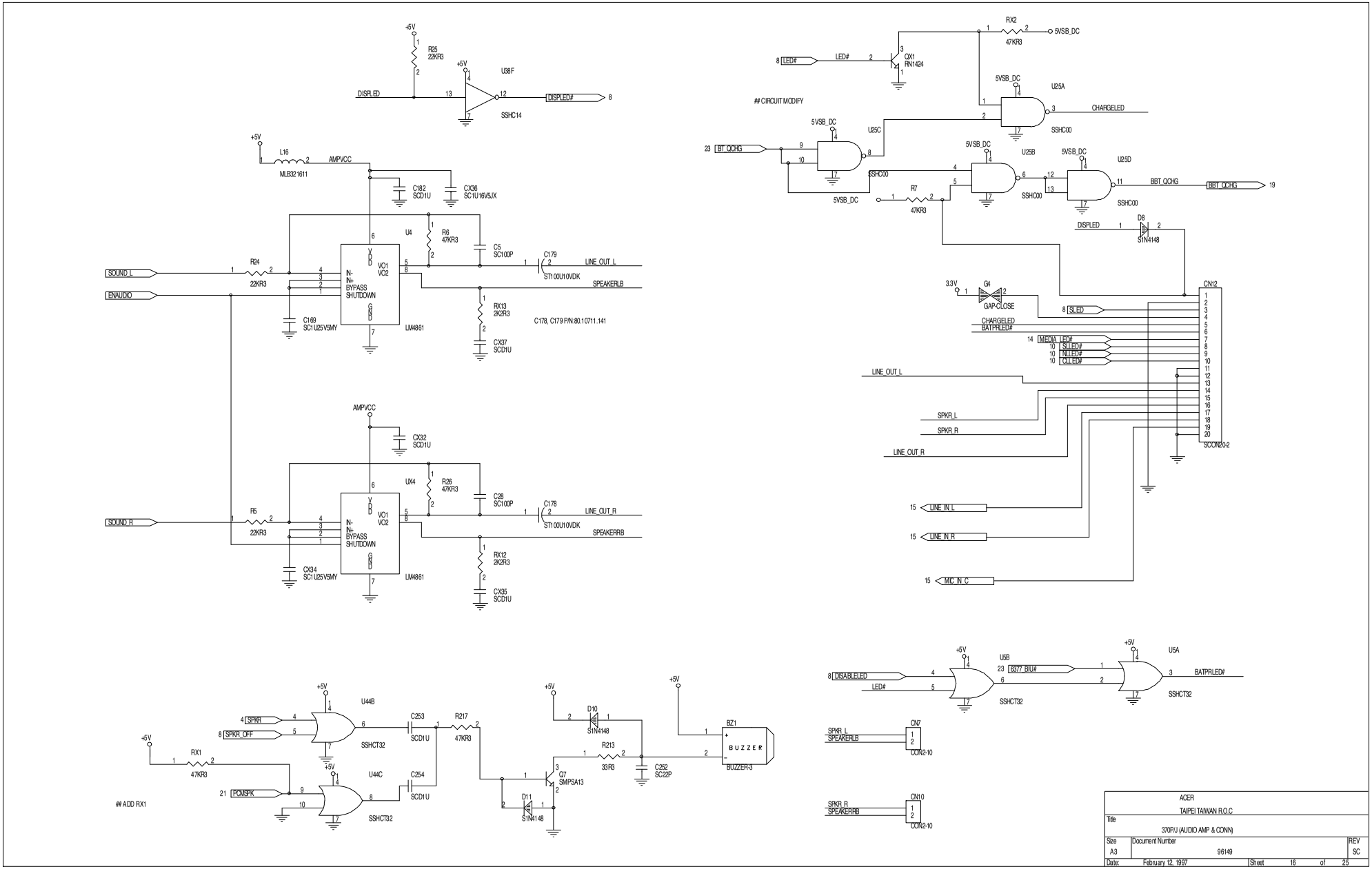
+5V
R25
22KR3
U8F
DISPLED
DISPLED#
SSHC14
L16
MLB321611
AMPVCC
C182
SCD1U
CX36
SC1U16V5JX
U4
R6
47KR3
C5
SC100P
C179
ST100U10VDK
LINE_OUT_L
SPEAKERLB
SOUND_L
R24
22KR3
ENAUDIO
C169
SC1U25V5MY
RX13
2K2R3
CX37
SCD1U
LM4861
C178, C179 P/N:80.10711.141
CX32
SCD1U
UX4
R26
47KR3
C28
SC100P
C178
ST100U10VDK
LINE_OUT_R
SPEAKERRB
SOUND_R
R5
22KR3
CX34
SC1U25V5MY
RX12
2K2R3
CX35
SCD1U
LM4861
RX2
47KR3
5VSB_DC
8 LED#
LED#
QX1
RN1424
CIRCUIT MODIFY
U25A
CHARGELED
SSHC00
U25C
23 BT_QCHG
U25B
U25D
BBT_QCHG
19
R7
47KR3
D8
DISPLED
S1N4148
3.3V
G4
GAP-CLOSE
CN12
8 SLED
CHARGELED
BATPRLED#
14 MEDIA_LED#
10 SLED#
10 NLED#
10 CLED#
LINE_OUT_L
SPKR_L
SPKR_R
LINE_OUT_R
SCON20-2
15 LINE_IN_L
15 LINE_IN_R
15 MIC_IN_C
U44B
4 SPKR
8 SPKR_OFF
SSHCT32
C253
SCD1U
R217
47KR3
RX1
47KR3
21 PCMSPK
U44C
C254
SCD1U
SSHCT32
ADD RX1
D10
S1N4148
R213
33R3
Q7
SMPSA13
D11
S1N4148
C252
SC22P
BZ1
BUZZER
BUZZER-3
U6B
8 DISABLELED
LED#
6377_BIU#
SSHCT32
U5A
BATPRLED#
SSHCT32
SPKR_L
SPEAKERLB
CN7
CON2-10
SPKR_R
SPEAKERRB
CN10
CON2-10
ACER
TAIPEI TAIWAN R.O.C
Title
370PJU (AUDIO AMP & CONN)
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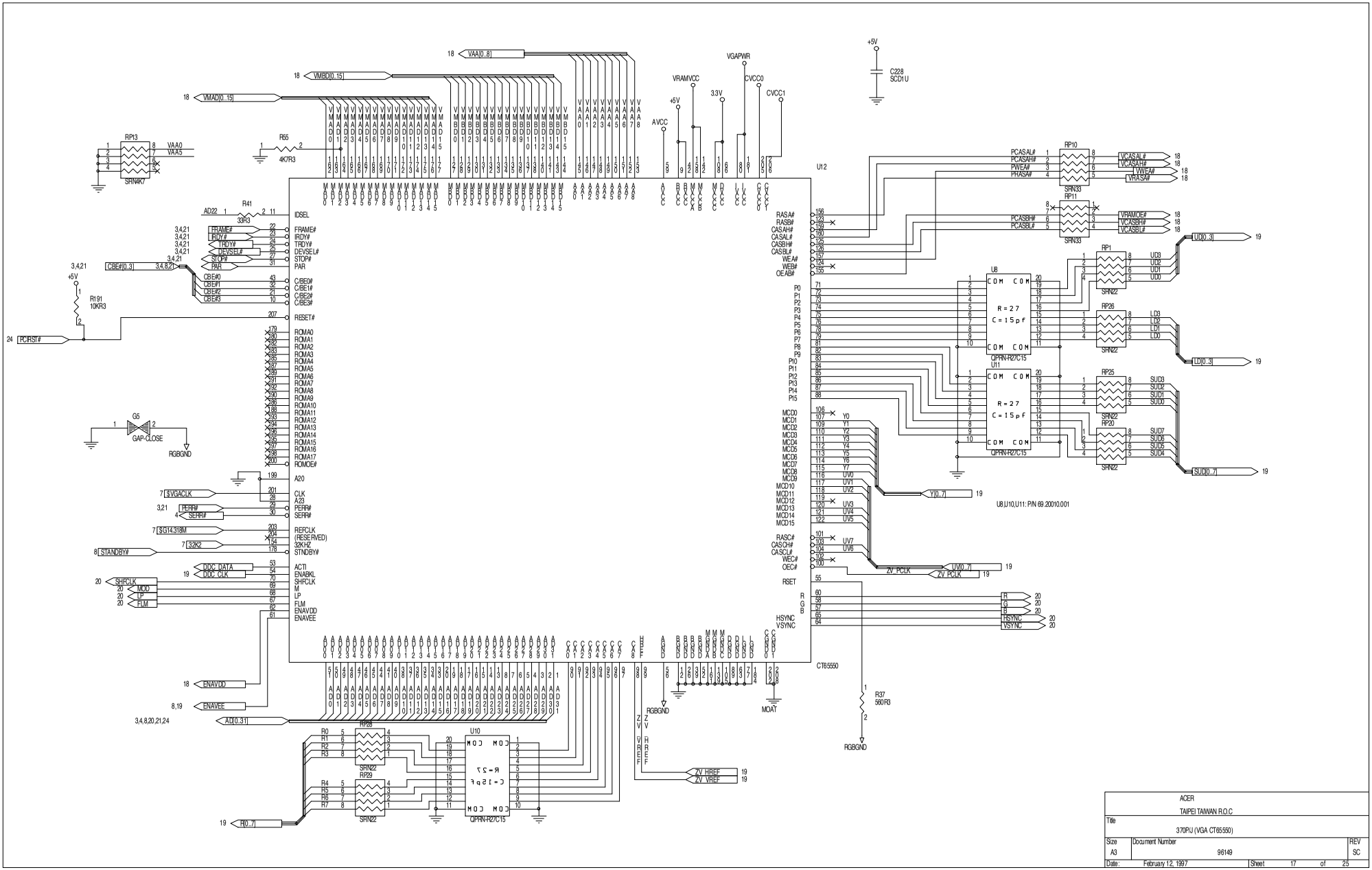
U12
CT65550
U8
U11
U10
QPRN-R27C15
U8,U10,U11: P/N 69.20010.001
ACER
TAIPEI TAIWAN R.O.C
Title
370PU (VGA CT65550)
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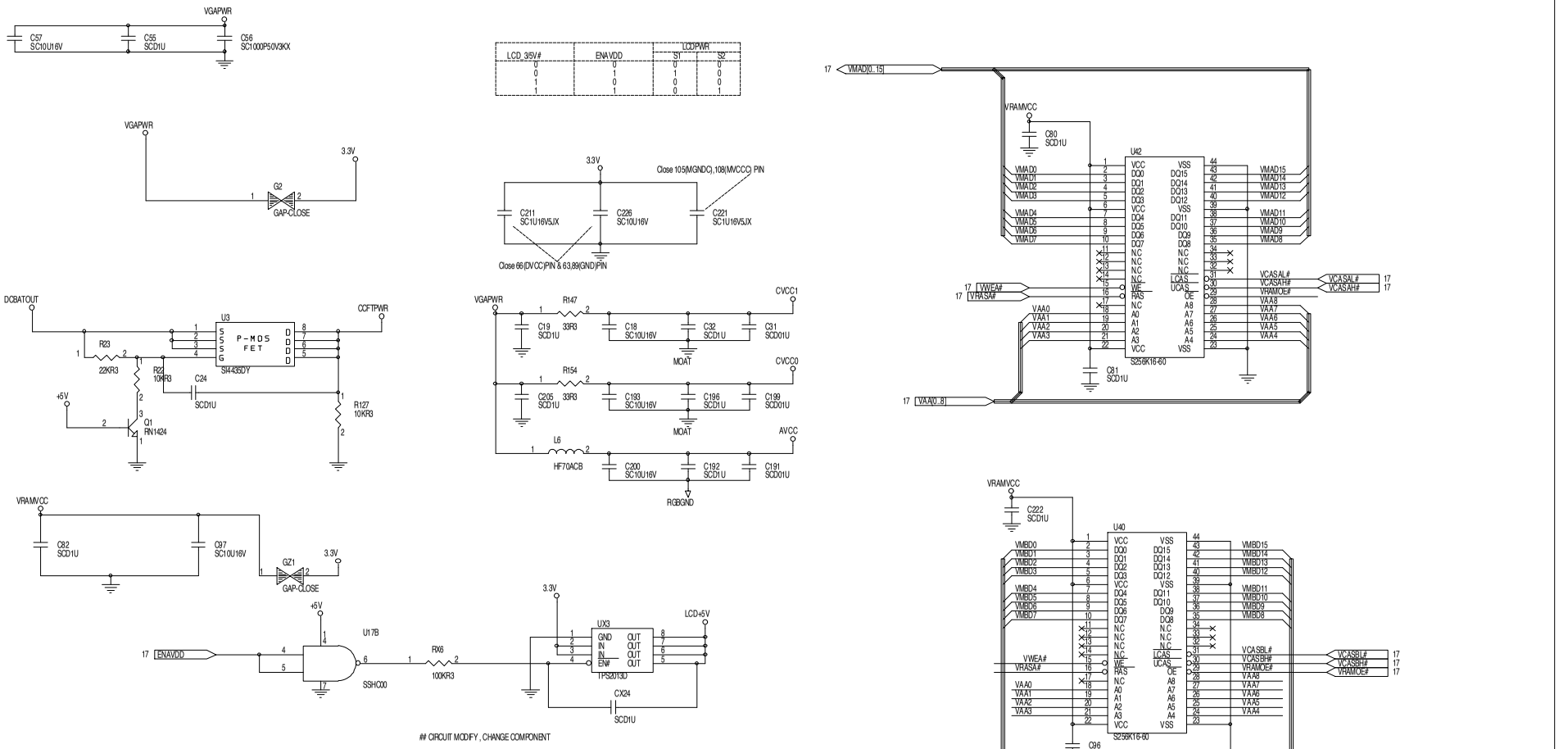

ACER	
TAIPEI TAIWAN R.O.C	
Title	370PJ (VRAM & VGA BYPASS CAPACITOR)
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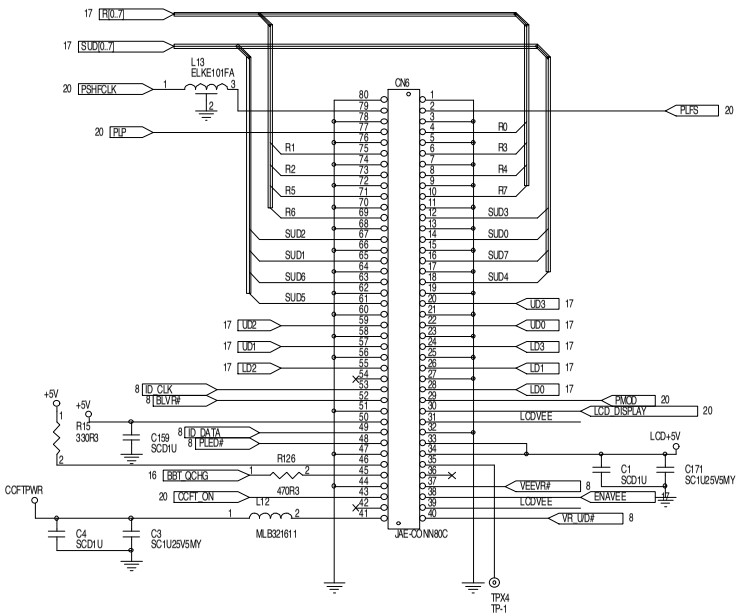
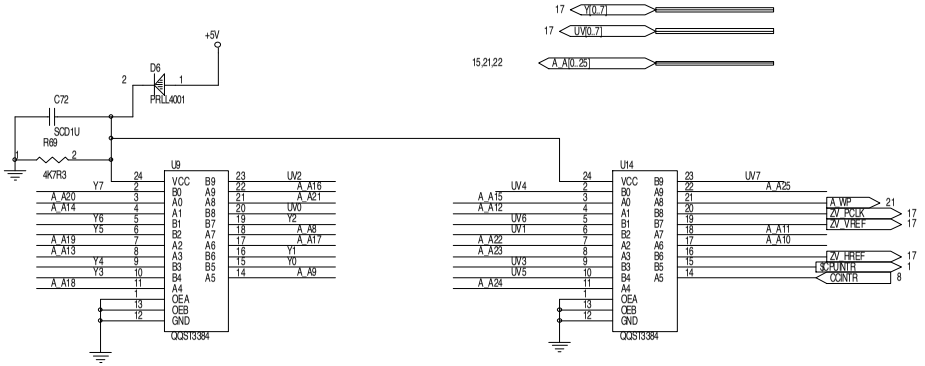
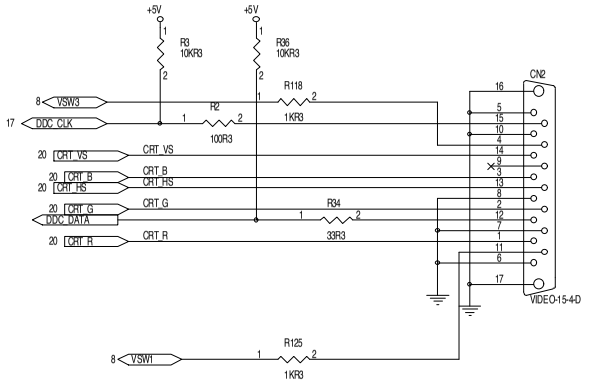


THIS CONN. IS LCD INTERFACE CONN.





ACER		
TAIPEI TAIWAN R.O.C		
Title	370PIJ (CRT CONN.& ZV PORT)	
Size: A3	Document Number: 96149	REV: SC
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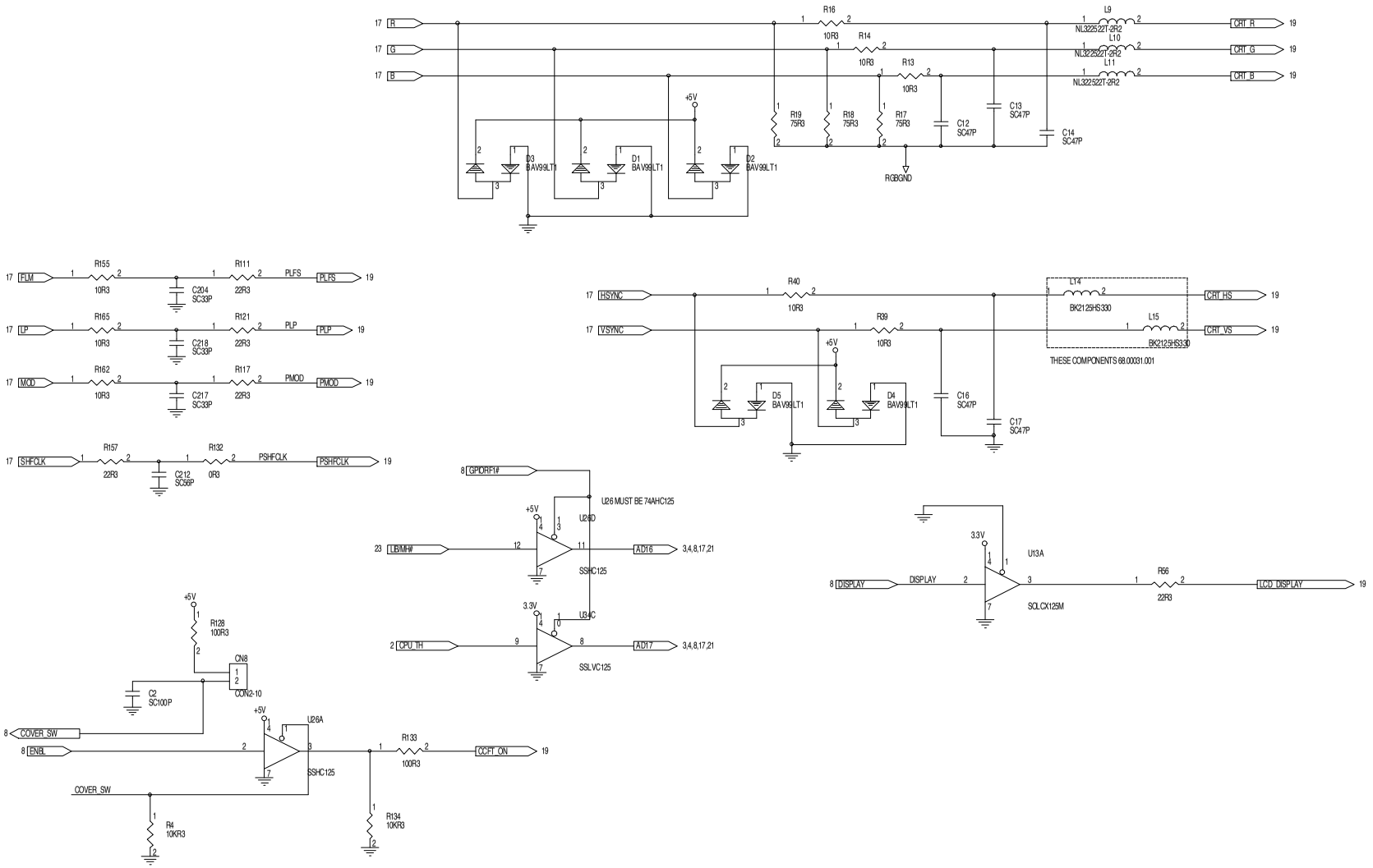

ACER		
TAIPEI TAIWAN R.O.C		
Title	370PJ (LCD I/F)	
Size: A3	Document Number: 96149	REV: SC
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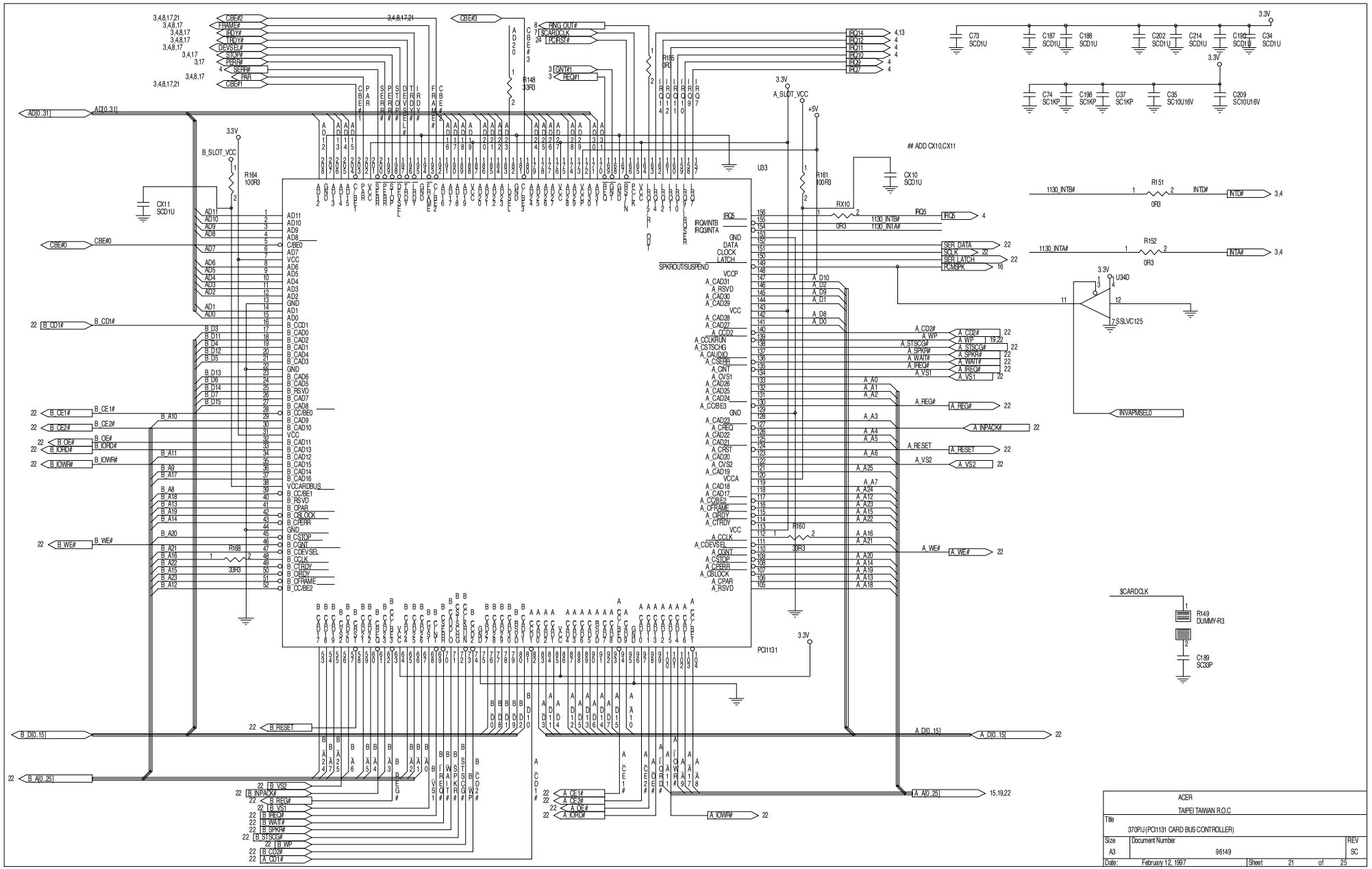
PCI1131
U33
U34D
SLVC125
R164 100R3
R161 100R3
R148 33R3
R160 33R3
R168 33R3
R165 0R3
RX10
R151 0R3
R152 0R3
R149 DUMMY-R3
CX1.1 SCD1U
CX10 SCD1U
C73 SCD1U
C187 SCD1U
C188 SCD1U
C202 SCD1U
C214 SCD1U
C190 SCD1U
C34 SCD1U
C74 SC1KP
C198 SC1KP
C37 SC1KP
C35 SC10U16V
C209 SC10U16V
C189 SC33P
ADD CX10,CX11
3.3V
+5V
B_SLOT_VCC
A_SLOT_VCC
AD[0..31]
B_A[0..25]
A_A[0..25]
B_D[0..15]
A_D[0..15]
$CARDCLK
INVAPMSEL0
ACER
TAIPEI TAIWAN R.O.C
Title
370PU (PCI1131 CARD BUS CONTROLLER)
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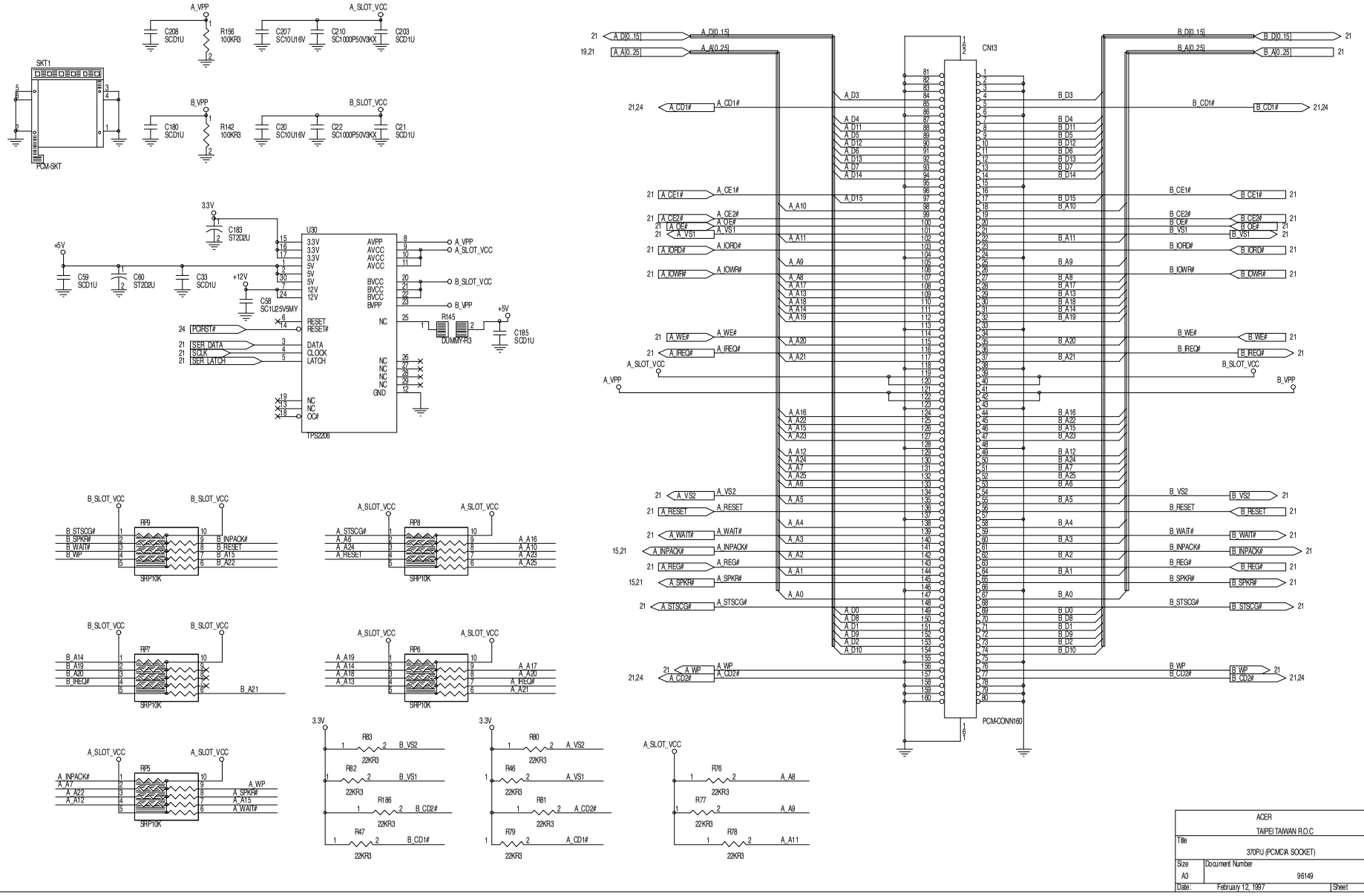

ACER			
TAIPEI TAIWAN R.O.C			
Title	370P/J (PCMCIA SOCKET)		
Size	Document Number		REV
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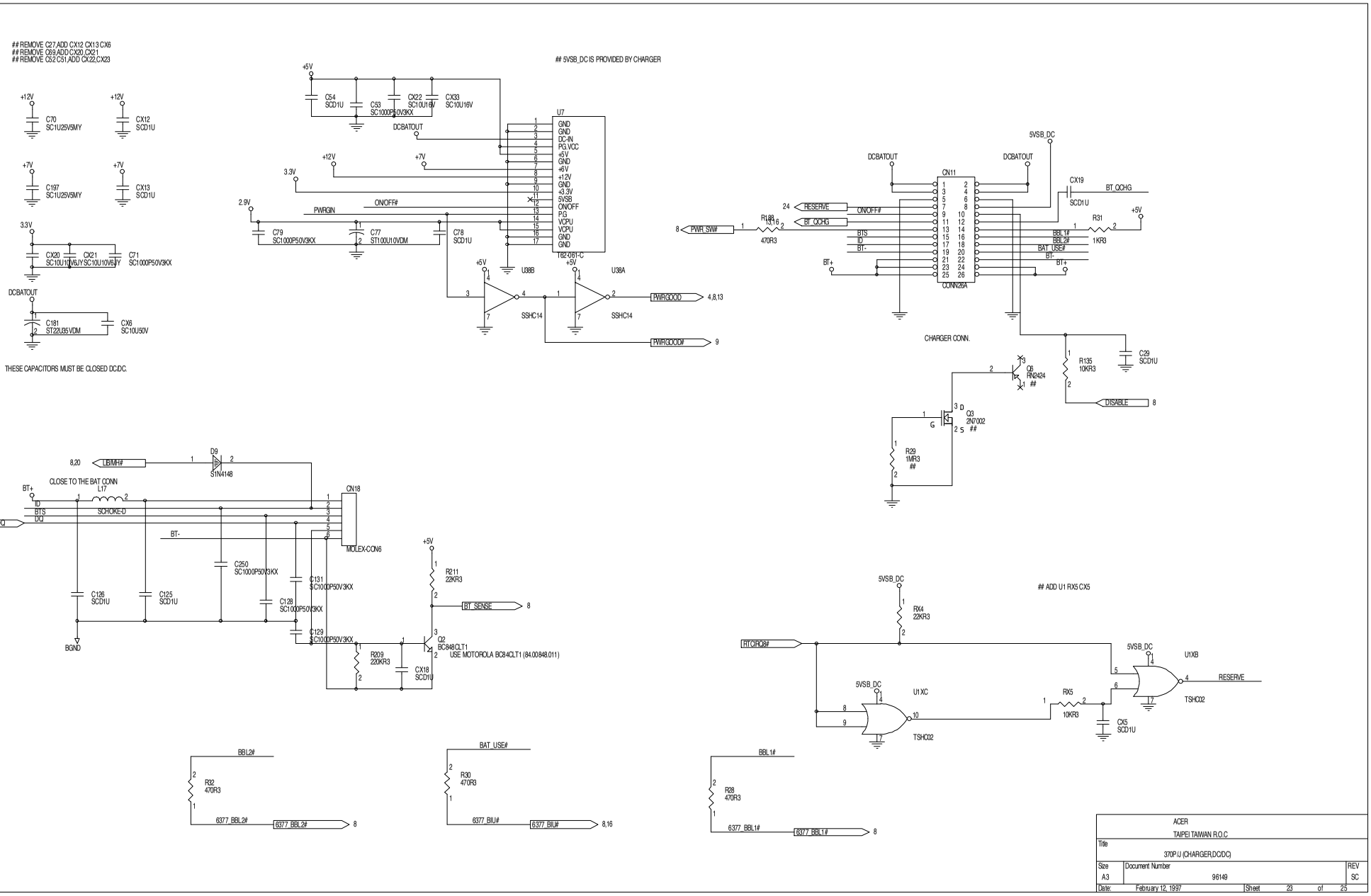
REMOVE C27,ADD CX12 CX13 CX6
REMOVE C69,ADD CX20 CX21
REMOVE C52 C51,ADD CX22,CX23
5VSB_DC IS PROVIDED BY CHARGER
THESE CAPACITORS MUST BE CLOSED DC/DC.
CHARGER CONN.
CLOSE TO THE BAT CONN
ADD U1 RX5 CX5
ACER
TAIPEI TAIWAN R.O.C
Title
370PJ (CHARGER,DC/DC)
Size
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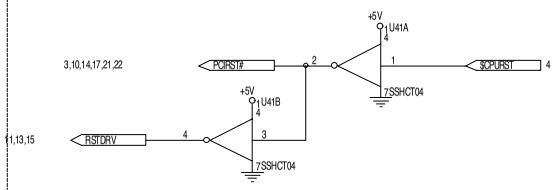
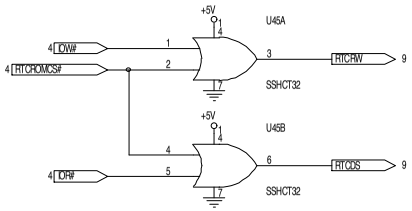
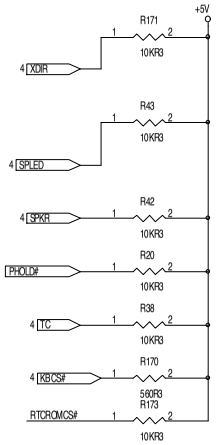
COMMON



POWER: VCC_IDE & GND



ALADDIN III



PULL L: 5V suspend mode enable.

PULL H: 5V suspend mode disable.

L: DMA DACK[7,5,3:0] polling enable.
*** If L, add ALDN3 P.21 MUX!
H: DMA DACK[7,5,3:0] polling disable.

L: Internal keyboard cntrler enable.

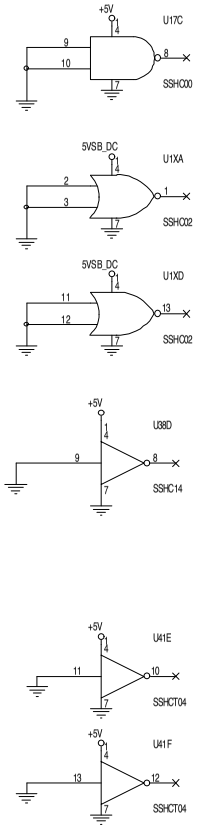
H: Internal KBC disable.

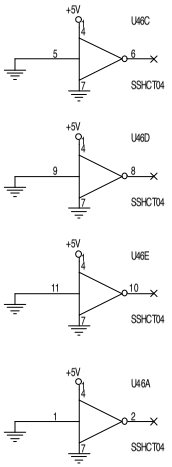
L: Internal RTC enable.
*** Refer to OKT down left.
H: Internal RTC disable.

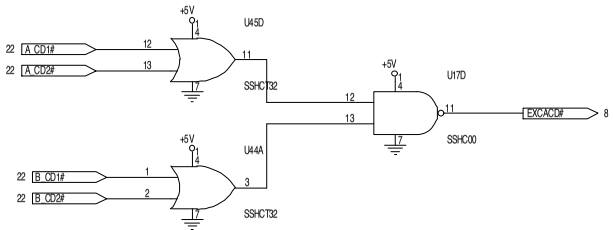
L: External I/O APIC mode supported.

H: Ext. I/O APIC mode not supported.

Must pull High.







ACER		
TAIPEI TAIWAN R.O.C		
Title: 370P/J (HW JUMPER SETTING)		
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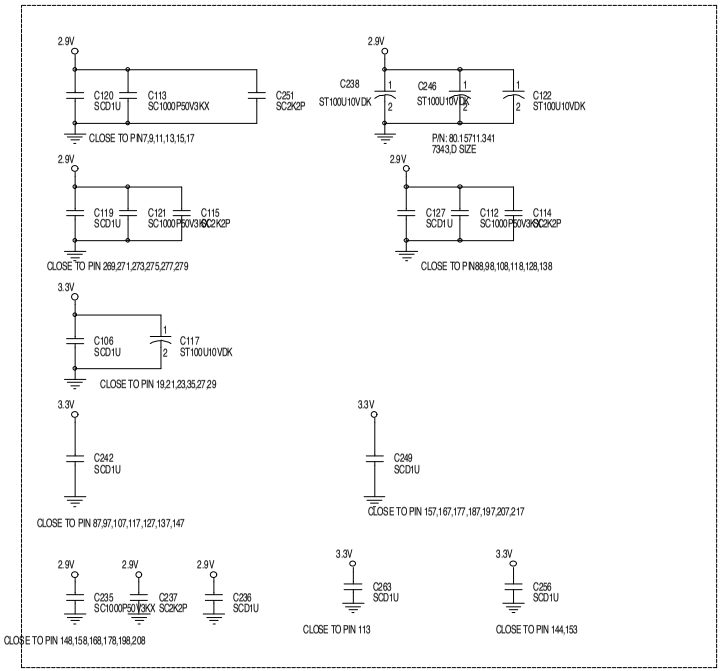
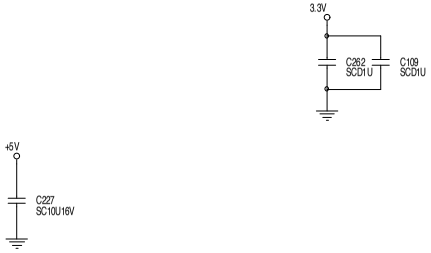
BYPASS CAPACITORS

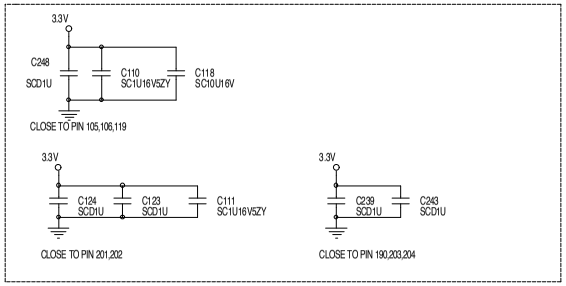
CPU



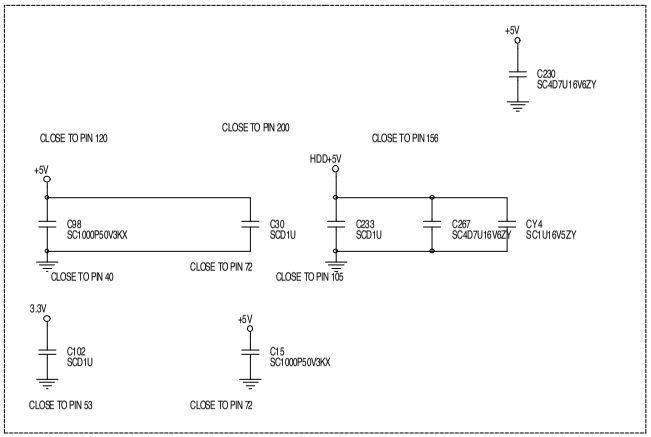
CACHE

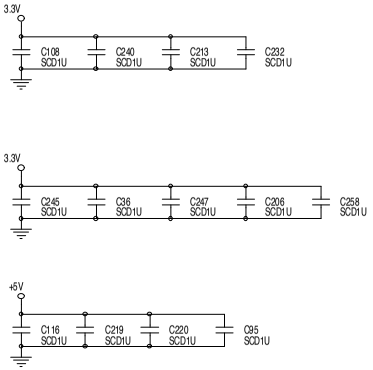


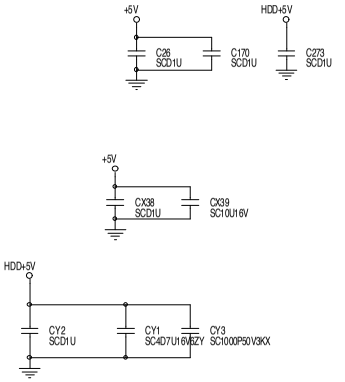
M1521



M1523







ACER		
TAIPEI TAIWAN R.O.C		
Title: 370PJ (BYPASS CAPACITORS)		
Size: A3	Document Number: 96149	REV: SC
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BIOS POST Checkpoints

This appendix lists the POST checkpoints of the notebook BIOS.

Table E-1 POST Checkpoint List

Checkpoint	Description
04h	• Check CPU ID • Dispatch Shutdown Path ***Note:*** *At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test is eliminated from the POST routine.*
08h	• Reset PIE, AIE, UIE ***Note:*** *These interrupts are disabled in order to avoid any incorrect actions from happening during the POST routine.*
09h	• Initialize m1511
0Ah	• Initialize m1513
0Bh	• Initialize m7101
10h	• DMA(8237) testing & initialization
14h	• System Timer(8254) testing & initialization
18h	• DRAM refresh cycle testing • Set default SS:SP= 0:400
1Ch	• CMOS shutdown byte test, battery, and check sum ***Note:*** *Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor is reset, therefore POST is re-entered. In order to prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point.* *The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly.* • Initialize default CMOS setting if CMOS bad • Initialize RTC time base ***Note:*** *The RTC has an embedded oscillator that generates 32.768 KHz frequency. To initialize the RTC time base, turn on this oscillator and set a divisor to 32768 so that the RTC can count time correctly*
1Dh, 1Eh	• DRAM type determination

Table E-1 POST Checkpoint List (Continued)

Checkpoint	Description
2Ch	• 128K base memory testing • Set default SS:SP= 0:400 ***Note:*** *The 128K base memory area is tested for POST execution. The remaining memory area is tested later.*
20h	• KB controller(8041/8042) testing • KB type determination • Write default command byte upon KB type
24h	• PIC(8259) testing & initialization
30h	• System Shadow RAM
34h	• DRAM sizing
3Ch	• Initialize interrupt vectors
4Bh	• Identify CPU brand and type
35h	• PCI pass 0
40h	• Assign I/O if device request
41h	• Assign Memory if device requested
44h	• Assign IRQ if device request
45h	• Enable command byte if device is OK
51h	• DownLoad keyboard matrix
50h	• Initialize Video display
4Ch	• ChipUp initialization for CPU clock checking
54h	• Process VGA shadow region
58h	• Set POST screen mode(Graphic or Text) • Display Acer(or OEM) logo if necessary • Display Acer copyright message if necessary • Display BIOS serial number
5Ch	• Memory testing
5Ah	• SMRAM test and SMI handler initialization
4Eh	• Audio initialization
60h	• External Cache sizing • External Cache testing(SRAM & Controller) • Enable internal cache if necessary • Enable external cache if necessary
64h	• Reset KB device • Check KB status ***Note:*** *The keyboard LEDs should flash once.*

Table E-1 POST Checkpoint List (Continued)

Checkpoint	Description
7Ch	• Reset pointing device • Check pointing device
70h	• Parallel port testing
74h	• Serial port testing
78h	• Math Coprocessor testing
80h	• Set security status
84h	• KB device initialization • Set KB led upon setup requests ***Note:*** *If keyboard Number Lock is enabled, the NumLock LED (if present) should be turned on.* • Enable KB device
6Ch	• FDD testing & parameter table setup ***Note:*** *The FDD LED should flash once and its head should be positioned*
88h	• HDD testing & parameter table setup
89h	• Get CPU MUX ***Note:*** *This routine is to identify the user-set CPU frequency, not CPU-required frequency*
90h	• Display POST status if necessary • Change POST mode to default text mode
93h	• Rehook int1c for quiet boot
94h	• Initialize expansion ROM • Shadow I/O ROM if setup requests • Build up free expansion ROM table
A4h	• Initialize security feature
A8h	• Setup SMI parameters
A0h	• Initialize Timer counter for DOS use
AAh	• m1523 modify
ACh	• Enable NMI • Enable parity checking • Set video mode
B0h	• Power-on password checking • Display configuration table • Clear memory buffer used for POST • Select boot device